Surface roughness exacerbated performance degradation in silicon nanowire transistors

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Scaling of silicon devices is fast approaching the limit where a single gate will fail to retain an effective control over the channel region. Of the alternative devices being researched, silicon nanowire transistors (SNWTs) show great promise in terms of scalability, performance, and ease of fabrication. In this work, the authors present the results of self-consistent, three-dimensional fully quantum mechanical simulations of SNWTs to show the role of surface roughness (SR) on the device parameter variation of SNWTs. The authors find additional quantum interference to take place when SR is taken into account in addition to a discrete impurity distribution. Due to this, the variations of the SNWT operational parameters increase about their mean value, indicating a performance concern. However, it is also seen that the quantum interferences are dependent on the dopant locations to a large extent, and for devices with preferential dopant configurations, these effects can be overcome to obtain nearly ballistic behavior. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2353846]

I. INTRODUCTION

The present scaling of silicon devices is fast approaching the limits where a single gate may become insufficient to retain an effective control over the channel region. Therefore, several new devices such as carbon nanotube field-effect transistors, double-gate and triple-gate metal-oxide-semiconductor field-effect transistors (MOSFETs), FinFETS, etc., which provide better gate control on the charge density in the channel, are being investigated. These devices have nonplanar architectures and have complex fabrication processes. Of these devices, trigate MOSFETs show great promise in terms of ease of fabrication with the existing technology, as well as device performance.[1] It has been shown that with proper design, trigate geometry is easier to manufacture than a fully depleted planar or double-gate structure.[2] The dimensions of the channel of these devices are of the order of tens of nanometers, and for all practical purposes, we may call these devices silicon nanowire transistors (SNWTs).

In the nanoscale regime, silicon on insulator (SOI) is preferred to bulk silicon (Si) as the buried oxide layer offers intrinsic isolation and, therefore, better scalability.[3] The width and the thickness of the Si body in these nanowire transistors are also aggressively scaled to maintain full depletion of the channel or to have a volume inversion in the intrinsic channel, as the case may be. Quantum mechanical confinement of carriers in these ultrasmall devices gives rise to interesting effects. While threshold voltage (V_T) increase due to confinement in the plane perpendicular to the interface is long known,[4] the increase of V_T due to confinement along the width of the device was shown in Ref. 5 for MOSFETs of width nearly 10 nm. This shows that for ultrasmall devices with dimensions of the order of few nanometers, the energies of the carriers are quantized in all three directions, and therefore theoretical understanding of the transport in such nanowire transistors can be obtained only by full three-dimensional (3D) quantum mechanical simulation.

The interface area of Si and silicon dioxide (SiO_2) increases with the increase of the number of gates in a MOSFET, and in a trigate structure, a larger fraction of carriers in the channel are exposed to the $Si-SiO_2$ interface than a planar structure. Therefore scattering from this surface can be a performance limiter for nanowire transistors. On the other hand, for a device with sufficiently small channel dimensions, one expects to have volume inversion of the channel for gate voltage (V_G) above V_T, and most of the electrons in such a case are expected to be in the center of the channel.[6] However, as devices are scaled down, the fraction of carriers that sees the interface area goes up, since the ratio of the interface area to the channel volume increases when the device is scaled down. This makes the situation interesting and shows the importance of considering surface roughness (SR) scattering in the simulation of these nanoscale device characteristics.

In this article, we report a self-consistent, fully 3D quantum mechanical simulation of a nanowire MOSFET built on an SOI substrate. We show that in such a device, the roughness at the $Si-SiO_2$ interface sets up additional interference that affect the transport of carriers, particularly in low and moderate fields. Besides, we show that the introduction of roughness at the interface changes the longitudinal states in the channel, and this in turn causes I_D of the device with SR to change. At still higher gate fields, the characteristics of the devices with and without SR come closer as the carrier energy is then sufficiently high to overcome the additional interference caused by the roughness.

II. DEVICE STRUCTURE

The device simulated here is a trigate *n*-MOSFET, built on an SOI wafer. Figure 1 shows a schematic of the device

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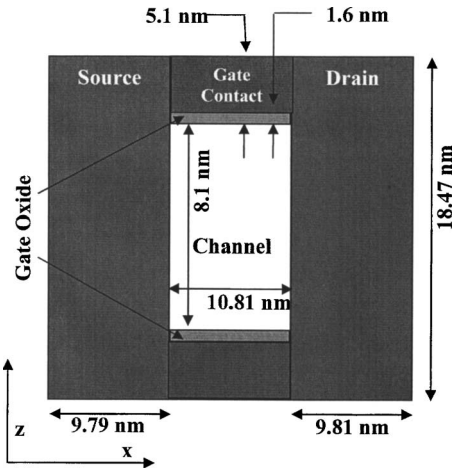

FIG. 1. Schematic of the simulated device, showing the device from the top. A 2 nm thick gate oxide sits on top of the channel region (not shown here), thus giving a trigate structure.

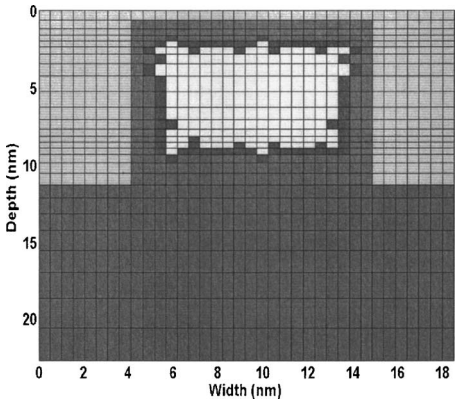

FIG. 2. Typical cross section of the simulated nanowire Si–SiO_2 interface, showing irregular interface generated by SR modeling.

geometry that we consider for this simulation. The channel region is *p* type and is left undoped. It is 10.8 nm long, 8.1 nm wide, and is surrounded by a 2 nm thick oxide on all sides. The crystal orientation of the channel is chosen such that the current flows along the ⟨100⟩ direction. The source and drain regions are large in size with length of 9.8 nm and width of 18.47 nm. In practical nanowire transistors, the source-drain regions, requiring external contacts, are large compared to the ultrasmall channel, and the interaction of the modes excited in the source with the channel constriction should be taken into account. The Si film is uniformly 6.51 nm high throughout the device. For such ultrasmall devices, the discrete nature of the dopants should be taken into account for a realistic treatment of the device, since the location of the ionized donor atoms significantly alters the potential landscape experienced by the carriers.[7] Therefore, the source-drain regions are *n* type doped with a nominal concentration of 10^{20} cm^{-3}, such that the dopants reside at discrete positions. This is done following an algorithm in which the Si region is traversed and a dopant is placed at a location if a generated random number exceeds the ratio of the nominal doping of that region to the volume of the Si atoms around that site.[7,8]

In this study, we model the Si–SiO_2 interface roughness using an exponential autocovariance function,[9] with rms roughness of 0.3 nm and correlation length of 1.3 nm. Though the values of these parameters will depend on the particular fabrication process, we assume here that the surface can be characterized by parameters having values similar to the case of dry oxidation of (100) Si.[9] SR is included by using a nonuniform mesh, with mesh spacing down to 0.36 nm at the interface, close to the scale of an atomic layer (~0.3 nm).[10] Thus the irregular nature of the interface is modeled without appreciably increasing the solution space. Figure 2 shows a vertical cross section of the device to illustrate a typical interface generated using this scheme.

Theoretical simulation of the role of SR scattering in SNWTs has earlier been reported in Ref. 11 and for a DG-MOSFET in Ref. 12. While Ref. 11 uses a finite element triangular mesh and an exponential autocovariance function to represent SR, the latter uses a linear discretization scheme along the Si–SiO_2 interface. Both of these simulators are based on the nonequilibrium Green's function formalism. While the former treats 3D effects, the latter is a two-dimensional simulator. In this work, we have used an efficient 3D recursive scattering matrix formalism based simulator reported in detail in Ref. 13, which is self-consistent and fully quantum mechanical in each direction. The carrier wave functions for each site are solved in this method, and the desired variables such as velocity, current, etc. can be obtained directly from the wave function.

We are interested in this work in the role of SR scattering and the discrete source-drain dopants on the device performance, where both of these processes tend to preserve the phase of the carriers. The temperature of all the simulations in this work is 300 K, and at this temperature, the inclusion of phonon scattering will overshadow the effects of the elastic processes. Therefore, in order to study the effect of the elastic processes on the ballistic transport of carriers, we have refrained from considering phonon scattering.

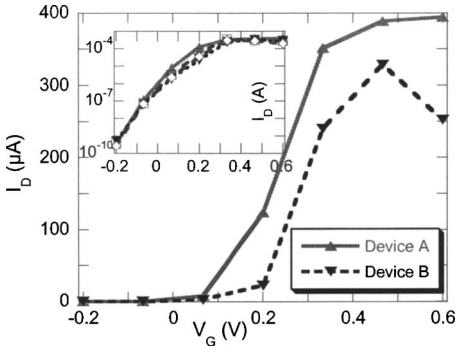

FIG. 3. I_D-V_G results in linear scale for the SNWT for two random dopant distributions, neglecting SR. V_D=0.6 V. Upper triangles (▲) denote the distribution which recovers nearly ballistic transport. Lower triangle (▼) represents the distribution that has most degraded performance due to strong quantum mechanical (QM) interference. Inset: I_D-V_G in log scale for four random dopant distributions, showing identical subthreshold characteristics.

TABLE I. Value of the SNWT operating parameters for various simulations. The same doping distributions are used for calculating parameters for rows 3 and 4 to investigate the effect of different SR patterns.

Parameters	(V_T) (mV)	ΔV_T (meV)	SS mV/decade	ΔSS mV/decade	I_{on}/I_{off}	$\Delta (I_{on}/I_{off})$
No SR Different dopant	93.1	9.53	68.08	2.28	692	107
Fixed SR Different dopant	127.5	19.1	70.33	2.43	741.38	145.24
No SR	99	⋯	67.71	⋯	897	⋯
Different SR Fixed dopant	144.9	2.5	68.79	0.39	1119	43.66

III. RESULTS AND DISCUSSION

A. Simulation of different dopant configurations

We first simulate the SNWT characteristics for four different random distributions of the dopants in the source-drain regions, without taking SR into account. The drain voltage (V_D) for all the simulations in this work is 0.6 V. The subthreshold behaviors of these devices are quite similar. This can be seen from the inset of Fig. 3, where I_D is plotted in a log scale as a function of V_G. However, on a linear plot considerable variation in I_D can be seen across the four devices, and this has been shown in Fig. 3 for two representative devices (device A and device B). Fluctuations in I_D caused by the discrete nature of doping have been reported earlier.[14–16] However, these results show that such variations are unavoidable, even when the channel region is undoped, and the dopants are confined to the source and drain regions. The mean value of the device operating parameters is calculated and shown in Table I along with the variations about the mean values. Since it is the variations rather than the absolute values that are of interest here, we use simple methods of calculation; e.g., V_T is calculated as V_G for which $I_D = 10^{-5}$ A; I_{on} and I_{off} are calculated for $V_G = 0.35$ and -0.05 V, respectively.

The dopant ions in the source and drain regions being positively charged cause the potential profile experienced by the electrons to alter dramatically, and this sets up points of interference. Stronger reflections are caused by dopants located near the source-channel interface. This causes device B to turn on later than others (▼ markers in Fig. 3). On the other hand, device A has few dopants close to the source-channel interface and exhibits nearly ballistic behavior (▲ markers in Fig. 3). The position of the dopant ions in the source and drain regions can be estimated from Fig. 4, where the black dots show the location of the dopant ions, and their relative size is varied such that dopants closer to the top interface appear bigger than those buried deep. Comparing the two figures, we can see a fewer number of dopants located near the source-channel interface in Fig. 4(a), and this explains the nearly ballistic I_D-V_G characteristic for the device. We wish to emphasize that the result reported here is unlike the reports (Refs. 15 and 16) that attribute the fluctuations of V_T to the fluctuation of channel charge caused by the dopant locations. Since our channel is undoped, the variations in I_D obtained from one device to another are a function

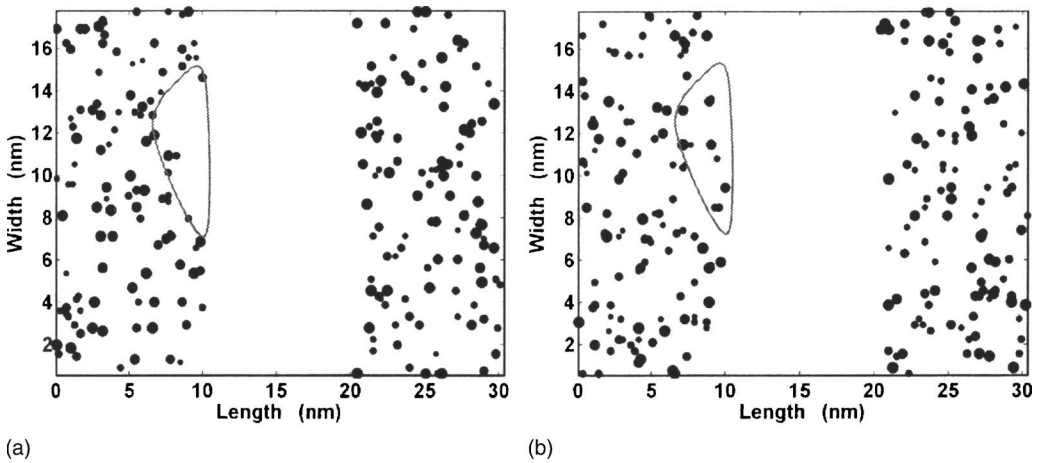

FIG. 4. Distribution of dopants in the source and drain regions. Larger dots represent dopants closer to the surface. Absence of dopants close to source-channel interface gives a nearly ballistic characteristic (▲ in Fig. 3). Dopants close to the source-channel interface set up strong QM interference, causing the large fluctuation in I_D (▼ in Fig. 3).

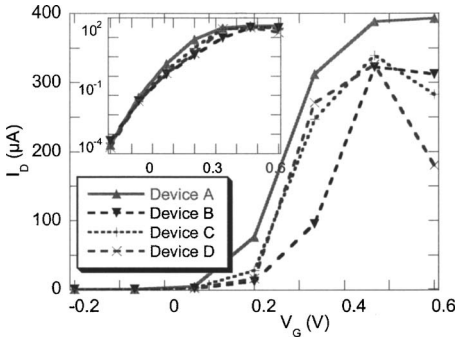

FIG. 5. I_D-V_G in linear scale for four different dopant distributions considering an identical SR pattern for each of them. Inset shows the same plot in log scale to show that subthreshold characteristics are equally affected.

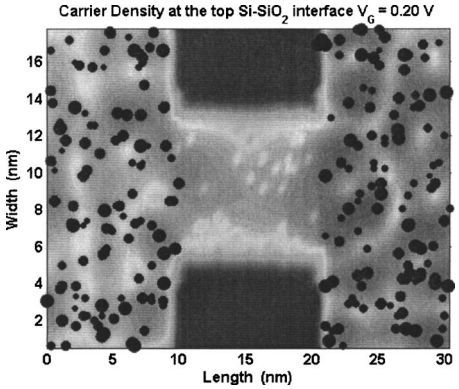

FIG. 6. Plot of the carrier density in the channel at a depth of 2.36 nm into the device. The effect of interface roughness can be seen in the fluctuation of the carrier density in the channel region. The black dots, representing dopant ions, are located only in the source-drain regions. Carrier concentration in the drain is higher as V_D=0.6 V, while V_S=0 V. V_G=0.2 V for this simulation.

of the interference effects of the dopant distributions in the source-drain regions, similar in nature to the fluctuations reported in Ref. 14.

The I_D-V_G results also show that the quantum interferences increase above threshold, leading to large variations in I_D across devices with different doping distributions. For $V_G > V_T$, the channel is sufficiently populated with electrons and the interference effects are stronger. A large number of dopants close to the interface in the source and drain regions cause the electron densities around these dopants to interfere destructively in the channel. With increase of V_G, the electron densities around these dopants increase, so that for certain dopant configurations, the destructive interference of the carrier density also increases, causing a decrease of carrier density in the channel with an increase of V_G. This leads to a corresponding decrease in I_D, and in turn explains the erratic I_D for device B in Fig. 3.

B. Effect of SR in devices with different dopant configurations

In Fig. 5, we show the I_D-V_G results for the same four dopant distributions, now including an identical SR pattern for all four devices. As before, we plot I_D-V_G in a log scale in the inset, showing similar subthreshold behavior across these devices, and a in linear scale in the main figure. In the subthreshold region, I_D is reduced when SR is included in the simulation, as the rough interface serves as an additional source of scattering. This increases the mean V_T, as can be seen from the parameter values in Table I. However, at high V_G, I_D characteristics of the devices vary widely from the "smooth" device (the device without considering SR) values. This shows that when the channel is populated, the interface roughness causes an additional interference over and above the quantum interference caused by the dopant ions. This causes a large spread in the device parameters (second row in Table I), indicating that SR reduces the control over device performance. Below threshold, when the channel is not sufficiently populated with electrons, SR cannot interfere effectively with the carrier density in the source region, and this causes comparatively similar subthreshold behavior across the devices. Nearly identical subthreshold slope (SS) with and without considering SR and a small value of the deviation (ΔSS) corroborate this reasoning. The deviation of I_D from that of the smooth device is particularly large for device B (black ▼ markers in Fig. 5), where the shallow dopant ions also happen to be in close proximity to a rough section of the top gate-oxide-channel interface. The carriers scattered from the interface get trapped in the potential field of the dopants in this case, thus aggravating the situation. This can be seen in Fig. 6, where the carrier density at the top of the channel, 2.36 nm down from the gate, is plotted for device B. The effect of the interface roughness on the self-consistent carrier density can be seen in the middle of the channel, and the aggregation of carriers near the dopant ions at the source-channel interface can also be discerned in Fig. 6.

It is interesting to note that for gate bias above threshold, for certain situations, it is possible to have a larger value of I_D for a device when including SR than for the case when the $Si-SiO_2$ interface is smooth. The inclusion of surface roughness changes the channel geometry as oxide is allowed to project into the channel, and similarly silicon can project into oxide. This shifts the longitudinal states that are available for the electrons to tunnel through from the source to the drain, and under constructive situations, this can give rise to a higher I_D for the device with SR than for a device without considering SR. However, this should not be thought of as an advantage, but an additional detrimental effect that causes an increase in the deviation of the device parameter values.

C. Simulation of different SR patterns in devices with identical dopant configuration

For the next simulation, we choose a dopant distribution corresponding to device D that has a moderate concentration of dopant ions located close to the source-channel interface, so that the I_D-V_G characteristics of the device is in between the extremes discussed in Sec. III A. Keeping this dopant distribution fixed, we simulate the device characteristics for four random SR patterns. A different seed is used for generating each of these surfaces, so that the rms roughness for these four different SR patterns is the same 0.3 nm, while the

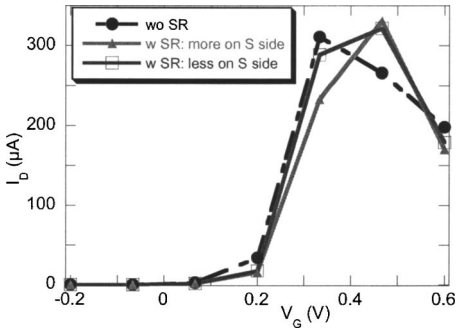

FIG. 7. I_D-V_G for the dopant distribution corresponding to device D (moderate number of dopants close to the source-channel interface). The dashed plot shows the curve without taking SR, and the solid lines are for two different SR patterns having the same rms roughness of 0.3 nm.

"rough" sections of the $Si-SiO_2$ interface are located at different positions along the channel. In Fig. 7, we plot the I_D -V_G results for the SNWT for two of these different SR patterns, along with the case where there is no SR. The two devices have been chosen such that one of them has more of the rough section close to the critical source-channel interface, and the other has less roughness in that region. The I_D-V_G characteristics of the devices with different roughness patterns are very similar to one another. We refrain from showing the subthreshold behavior, as in a log scale; all of them appear almost one on top of the other. Each of these different SR patterns causes reduction of I_D with an attendant increase of V_T. We also find that the SS remains nearly constant, while the I_{on}/I_{off} ratio increases. This is due to the fact that SR scattering is more effective for carriers in the low field regime, and this reduces I_{off} more than I_{on}, and therefore the ratio I_{on}/I_{off} increases, when compared to a smooth device. These findings are summarized in Table I. Up to a bias V_G=0.33 V, I_D values are what one would expect usually, namely, I_D for the smooth device is largest, followed by the device that has comparatively less rough section near the source-channel interface. However, at V_G=0.47 V, the trend is reversed because of the shift of the longitudinal states due to the inclusion of SR. This again shows that under constructive situations, the interference caused by the rough surface can result in a larger I_D value compared to the device which has a smooth interface. At still higher V_G, the drain current of the device becomes almost identical, with or without taking SR into account, as the energy of the carriers at this bias is sufficient to overcome the interference caused by SR scattering.

IV. CONCLUSION

A self-consistent 3D fully quantum mechanical simulation of a SNWT has been done to investigate the effect of SR on the device performance. It is seen that below threshold voltage, SR reduces I_D by increasing the scattering in the channel, causing V_T to increase slightly. For higher V_G, SR serves to modify the quantum interference of carriers with the discrete dopant ions, thereby setting up additional fluctuations in I_D. The variation of the device operating parameters due to the discrete dopant locations in the source-drain regions is further exacerbated by this additional quantum interference due to the rough interface. This suggests that a certain degree of control of the position of the dopant locations, even in the source-drain regions, is necessary to maintain the uniformity of device characteristics for these nanoscale transistors. However, it is also heartening to note that if the dopant ions can be kept somewhat away from the source-channel interface, the current is not significantly degraded, and a nearly ideal behavior can be recovered. Even when the dopants are present near the source-channel interface, if they are buried deep inside the silicon, the quantum interference with the rough section of the interface is comparatively low, and this in turn will cause less variation of the SNWT operating parameters. Thus this study underscores the importance of keeping the dopants away from the source-channel interface and the oxide-silicon interface to achieve uniformity in values of operating parameters across a large number of devices.

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