J Comput Electron (2007) 6:141–144
DOI 10.1007/s10825-006-0086-6

Phonon exacerbated quantum interference effects in III-V nanowire transistors

M. J. Gilbert · S. K. Banerjee

Published online: 18 January 2007

Abstract In recent years, a great deal of attention has been focused on the development of quantum wire transistors as a means of extending Moore's Law. Here we present, results of fully three-dimensional, self-consistent quantum mechanical device simulations of InAs tri-gate nanowire transistor (NWT). The effects of inelastic scattering have been included as real-space self-energy terms. We find that the position of dopant atoms in these devices can lead a reduction in the amount of scattering the carriers experience. We find that the combination of deeply buried dopant atoms and the high energy localization of polar optical phonon processes allow devices to recover their ballistic behavior even in the presence of strong inelastic phonon processes. However, we find that dopant atoms close to the source-channel interface cause severe quantum interference effects leading to significant performance reduction.

Keywords MOSFET · Quantum wire · Transport · Simulation

Introduction

It has been a well established fact that the semiconductor industry must devise an alternative solution to the bulk silicon MOSFET in order to continue the relentless scaling of device density. One of the most promising of these new technologies is the quantum wire MOSFET. Tri-gate devices offer greatly improved electrostatic control over the channel of the device when compared to the traditional MOSFET due to the presence of the additional gates [1]. With a device of this nature, it is necessary to use a simulation tool that takes into account the quantum confinement in the system. Previously, one only had confinement in the direction perpendicular to the gate, but the width of the channel is now on the order of the Fermi wavelength of the electron. There have been many different simulations of ballistic operation of these devices [2–3]. However, recent work has shown that there is limited applicability to the assumption that in at channel lengths of ∼10 nm the nature of the transport is ballistic [4]. Therefore, while examination of the ballistic limit may provide an interesting baseline, we must include the role of scattering.

Within the last few years, there has been a renewed interest in the use of III-V materials instead of silicon for future generation transistors. Previous studies have shown that care must be taken in the fabrication of these devices or large increases in the output drain current (kink effect) occur [5–6]. Through the use of quantum wires with discrete subbands for the active regions of the device, the kink effect may be eliminated. Nevertheless, there has been interest in MOSFETs in these III-V materials for use in high speed logic applications [7].

In this paper, we present the results of a three-dimensional, self-consistent, quantum mechanical device simulation of several tri-gate InAs quantum wire MOSFETs. Here we present results of 10 nm channel length devices both in the elastic limit, where we only include interactions with the dopant ions, and with both elastic and inelastic effects (the effects of impurity, acoustic deformation potential, intervalley ($\Gamma\rightarrow$ X and $\Gamma\rightarrow$L) and, polar optical phonon (POP) scattering as separable real space self-energy terms). We show that the inclusion of inelastic phonon processes does not have a significant effect on the InAs devices. This is due to the fact that the POP process becomes highly localized in space as the carriers gain energy leading to reduced

M. J. Gilbert (✉) · S. K. Banerjee
Microelectronics Research Center, University of Texas at Austin, Austin, TX 78758
e-mail: mgilbert@mer.utexas.edu

scattering rates. Thereby, allowing the devices to regain ballistic characteristics.

Device structure and method

The thickness of the InAs layer is 9.09 nm. The source and drain of the device are *n*-type with a doping density of $6 \cdot 10^{18}$ cm^{-3}, while the channel of the device is considered to be *p*-type, but undoped. The gate material is assumed to be platinum and the gate oxide on each side is composed of 1 nm of hafnium oxide (HfO_2). Underneath the device, we have assumed a generic insulating substrate. The structure of the device with the 9.69 nm channel is exactly the same with the exception, of course, of the channel length. Once the device geometry is defined, the InAs lattice is scanned and the dopants are distributed according to the method presented in [8]. The exact device dimensions (multiples of the lattice constant) have been included in this simulation to aid in the inclusion of the discrete dopants. Following the distribution of the dopants, they are then mapped back onto the grid of the simulation mesh and the initial self-consistent Poisson solution is obtained. In this case, the full Coulomb potential of the dopants is incorporated. Then, the solution of Poisson's equation for the local potential is no longer smoothly varying in the source and the drain of the device. The inclusion of discrete dopants causes the formation of potential variation in the source and drain. The density throughout the device is calculated using a variant of the recursive scattering matrix method which solves the Schrödinger equation in the effective mass approximation as described in [2]. In short, this method provides us with a three-dimensional, fully quantum mechanical method. Since the transport calculation is performed in real space, the different excited modes in the system are automatically coupled unlike in other simulations [3]. In order to achieve self-consistency, the density obtained from the transport calculation is then updated using Broyden's method [9] and a new guess for the potential is obtained through the solution of Poisson's equation. The process is repeated until a desired level of convergence is obtained. Exchange and correlations terms are included through a local density approximation [10]. All of the simulations are performed at 300 K and a static drain current of $V_d = 0.6$ V is applied. Each of the scattering mechanisms mentioned in the introduction is included in the simulation as a real-space self-energy term in the Hamiltonian [4, 11]

Results and discussion

In Fig. 1, we plot the I_d-V_g curve for two discretely doped tri-gate InAs quantum wire devices with only elastic (boundary and impurity) scattering considered. Speaking in terms

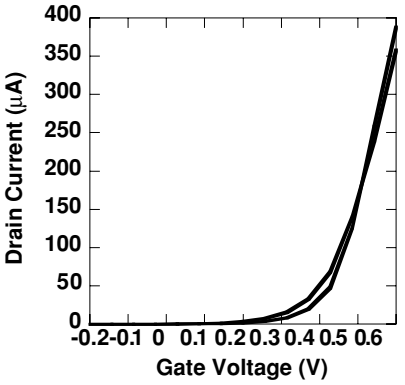

Fig. 1 I_d-V_g curves with only elastic scattering processes included

of simple device performance, averaging over 4 different devices, we find that the threshold voltage is found to be 0.373 V $\pm$ 11 mV. These figures are slightly different from those quoted elsewhere [12], but it should be noted that we have used a smaller sampling of devices in this study. While the threshold voltage is, at present, too high for next generation technology, with the use of gate stack engineering [12] this figure can be brought down to acceptable levels. Further, we see that the spread in the threshold voltage is quite small. This is due to the fact that fewer dopant atoms are required to reach these levels of performance. Thus, with fewer elastic scattering sights to induce quantum interference, the threshold voltage is expected to be more stable than in its silicon based equivalents.

In Fig. 2, we utilize one dopant distribution and now include the phonon processes in addition to the electron-impurity interactions. Due to the fact that in InAs the X and L valleys are offset from the Γ valley by large energy offsets, the contribution of intervalley scattering will typically be quite small for the voltages applied to the device here. By limiting the effectiveness of the intervalley processes, and with the already small acoustic deformation potential scattering, we

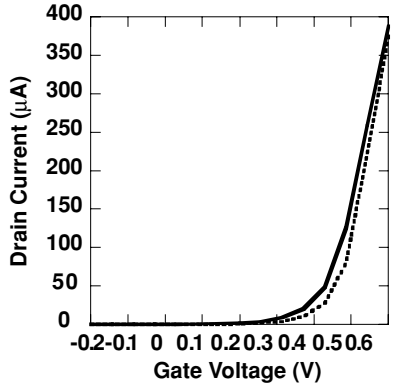

Fig. 2 I_d-V_g curves for elastic scattering processes (solid) and a combination of elastic and inelastic scattering (dotted) included for deeply buried dopants

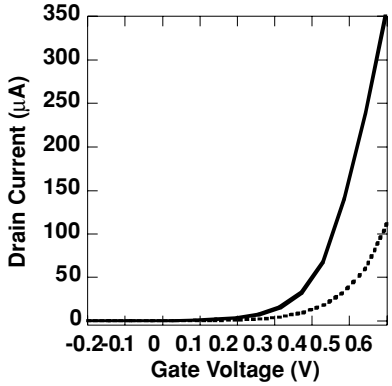

Fig. 3 I_d-V_g curves for elastic scattering processes (solid) and a combination of elastic and inelastic scattering (dotted) included for dopants near the source-channel interface

find a situation where basically the only inelastic process is that of POP scattering. Examining the curves, we find that in the low gate voltage regime POP scattering significantly reduces the current. This shift in low gate voltage current leads to modifications to the performance. The threshold voltage averaged over four devices is 0.423 V $\pm$ 7 mV. Based on this result, we find that the POP scattering does indeed shift the threshold voltage, but it also stabilizes this device measure by reducing spread in carrier energy in the source.

At high gate voltages, we find that the current in both the elastic and combined (elastic scattering contribution + inelastic scattering contribution) cases that the drain currents begin to merge after $V_g = 0.5$ V. This can be most directly attributed to a high energy localization of the POP scattering rate. This localization reduces the scattering rate as less of the non-local contribution influences the rate. Therefore, the inelastic perturbations to the current tend to become negligible and we are left only with the elastic interactions.

While in Fig. 2 the majority of the dopant atoms were buried allowing the device to recover quasi-ballistic behavior, in Fig. 3, we plot the I_d-V_g curves corresponding to a single discretely doped device with elastic (solid) and inelastic plus elastic interactions (dotted). Now the locations of the dopant atoms are such that in the source of the device there are two dopant atoms near the entrance to the channel in the middle of the semiconductor layer. These dopant atoms cause significant modifications to the energy of the incident electrons. The lower energy electrons now see heavier POP scattering which, when combined with the typical reflections from the channel entrance, gives rise to significant reductions in the amount of charge in the channel. With less conduction in the channel, the device sees significantly degraded performance.

In Fig. 4, we plot the electron densities taken at depths of approximately 5 nm into the InAs device layer. The black dots in the figure represent the locations of the dopant atoms in the system. Dots that are larger in size are closer to the surface of the device, while dots that are smaller are buried farther

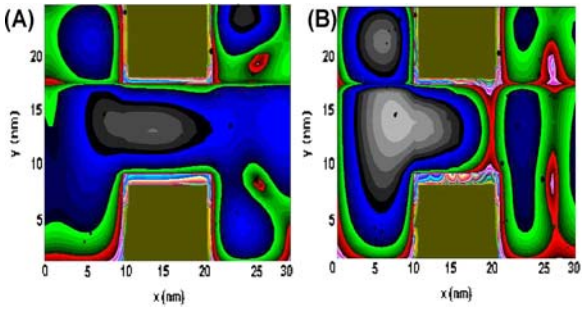

Fig. 4 Electron density in the *xy*-plane taken at a depth of approximately 5 nm into the InAs device layer for (a) elastic and (b) combined processes

down in the device. In Fig. 4(a) we plot the density at $V_g = 0.6$ V for the elastic case. At this voltage, we are clearly above the threshold voltage for the device. The channel is now fully populated with carriers. In the source and drain, the location of the electron density depends rather weakly on the locations of the dopants. This is mainly due to the scarcity of the dopants and that they are buried deeply in the InAs substrate which reduces their effect on the propagating electrons. Nevertheless, the density tends to roughly follow the path of the dopants as it makes its way to the channel. In the channel, we find that the some of the density has been trapped by multiple sequential reflections off of the source-channel and channel-drain interfaces. As the density then exits the channel, it begins to populate sites in the drain that are energetically preferential.

In Fig. 4(b), we plot the density at $V_g = 0.6$ V for the combined case. We see very distinct differences in the location and magnitude of the electrons in the combined case, but, in general, it follows the same general trend as in the elastic case. With the combined case, we find that there is a pronounced buildup of charge in the area of the source near the channel entrance of 0.38 k_bT. The reflection off of this interface alters the energy of the carriers to the point where some of the lower energy modes will see increased scattering and a reduction in density of approximately 0.25 k_bT in most areas. In the source, we find additional discrepancies as this is the location where the scattering is most prevalent. In the channel and drain of the device, we find that there is a corresponding reduction of electron density as much of the incident density has been reflected at the channel interface.

Conclusions

We have presented results of three-dimensional, self-consistent quantum device simulations. We find that in devices with deeply buried dopant atoms the inclusion of inelastic processes has a non-negligible effect on the device performance at low gate voltages leading to shifts in

the threshold voltage. This result is due mainly to the POP scattering effect as the quantum interference generated by the discrete dopants is minimized due to their location away from the charge centroid. At higher gate voltages, we find that the POP scattering switches from an inherently non-local process to a local one which allows the device to recover quasi-ballistic behavior. However, we see that the location of the discrete dopants in the device plays a profound role in determining the device performance. When dopant atoms are close to the channel interface, we find that the interaction shifts energies of some of the carriers to lower energies where they experience strong POP scattering severely degrading the device performance.

References

1. Doyle, H.S., Datta, S., Doczy, M., Hareland, S., Jin, B., Kavalieros, J., Linton, T., Murthy, A., Rios, R., Chau, R.: IEEE electron. Dev. Lett. **24**, 263 (2003)
2. Gilbert, M.J., Ferry, D.K.: J. Appl. Phys. **95**, 7954 (2004)
3. Wang, J., Polizzi, E., Lundstrom, M.: J. Appl. Phys. **96**, 2192 (2004)
4. Gilbert, M.J., Akis, R., Ferry, D.K.: J. Appl. Phys. **98**, 094303 (2005)
5. Boos, J.B., Krupps, W., Park, D., Molnar, B., Bennett, B.R.: Elect. Lett. **32**, 688 (1996)
6. Bolognesi, C.R., Caine, E.J., Kroemer, H.: IEEE Elect Dev. Lett. **15**, 16 (1994)
7. Chau, R., Datta, S., Doczy, M., Doyle, B., Jin, B., Kavalieros, J., Majumdar, A., Metz, M., Radosavljevic, M.: IEEE Trans. Nanotech. **4**, 153 (2005)
8. Gilbert, M.J., Ferry, D.K.: Superlatt Microstruct **34**, 277 (2003)
9. Johnson, D.D.: Phys. Rev. B **38**, 12807 (1988)
10. Wang, Y., Wang, J., Guo, H., Zaremba, E.: Phys. Rev. B **52**, 2738 (1995)
11. Gilbert, M.J., Ferry, D.K.: J. Phys. Conf. Series. Accepted for publication
12. Gilbert, M.J., Ferry, D.K.: J. Appl. Phys. **99**, 054503 (2005)