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Effect of elastic processes and ballistic recovery in silicon nanowire transistors

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Abstract Scaling of silicon devices is fast approaching the limit where a single gate may fail to retain effective control over the channel region. Of the alternative device structures under focus, silicon nanowire transistors (SNWT) show great promise in terms of scalability, performance, and ease of fabrication. Here we present the results of self-consistent, fully 3D quantum mechanical simulations of SNWTs to show the role of surface roughness (SR) and ionized dopant scattering on the transport of carriers. We find that the addition of SR, in conjunction with impurity scattering, causes additional quantum interference which increases the variation of the operational parameters of the SNWT. However, we also find that quantum interference and elastic processes can be overcome to obtain nearly ballistic behavior in devices with preferential dopant configurations.

Keywords Nanowire MOSFETs · Quantum interference · Discrete dopant effects · Surface roughness · Ballistic transport

1 Introduction

The present scaling of silicon devices is fast approaching the limit where a single gate may become insufficient to retain effective control over the channel region. Therefore, extensive research is going on for non-planar devices like double-gate and triple-gate metal-oxide-semiconductor field-effect transistors (MOSFETs), FinFETS, etc. which allow better gate control over the charge density in the channel. Of these, tri-gate MOSFETs show great promise in terms of ease of fabrication with existing technology, as well as device performance [1, 2]. The dimensions of the channels of these devices are of the order of tens of nanometers, and for all practical purposes, it is fair to refer to these as silicon nanowire transistors (SNWTs).

In the nanocale regime, silicon-on-insulator (SOI) is preferred to bulk silicon (Si) as the buried oxide (BOX) layer offers intrinsic isolation, and therefore better scalability [3]. The width and thickness of the silicon body of these nanowire transistors are also aggressively scaled, so that the energies of the carriers are quantized in all three directions, and therefore theoretical understanding of the transport in such nanowire transistors can be obtained only by full three-dimensional (3D) quantum mechanical simulation.

The Si and silicon-dioxide (SiO_2) interface area increases with increasing number of gates in a MOSFET. In a tri-gate structure, a larger fraction of carriers are exposed to the interface than in a planar structure. Therefore SR scattering can be a performance limiter for nanowire transistors. On the other hand, for a device with sufficiently small channel dimensions, one expects to have volume inversion of the channel for gate voltage (V_G) above threshold (V_T), and the electrons are expected to be in the center of the channel [6], away from the interface. These two competing factors make the situation interesting, and call for a detailed study of SR scattering on the performance of these nanoscale device characteristics.

In this work, we report a self-consistent, fully three-dimensional (3-D) quantum mechanical simulation of a tri-gate MOSFET built on an SOI substrate. Large fluctuations are observed in the drain current (I_D) of such a device due to the interference caused by the discrete dopant ions. We show that the roughness at the Si-SiO_2 interface sets up an additional interference that changes the longitudinal states in the channel, and this in turn causes a change in the I_D of

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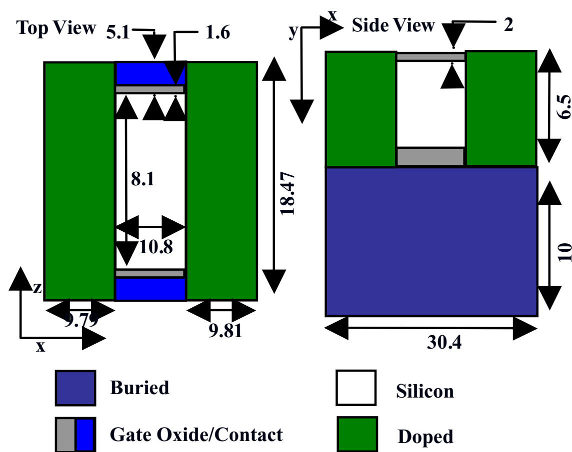

Fig. 1 Schematic of the simulated device, showing – at left, the device from top, and at right, a vertical cross-section through the middle of the device. All dimensions shown are in nm

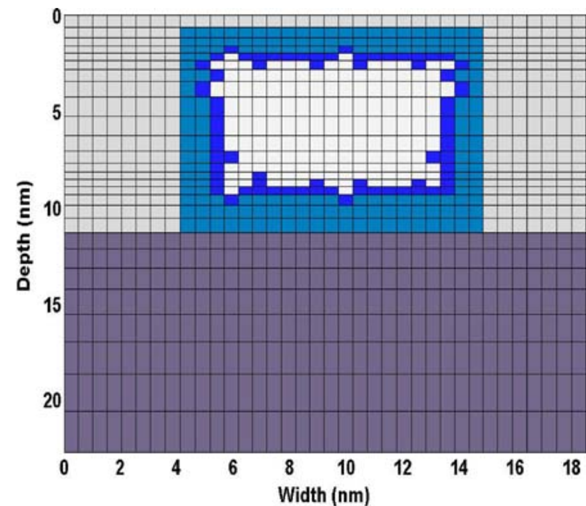

Fig. 2 Typical cross-section of the simulated nanowire Si-SiO_2 interface, showing irregular interface generated by SR modeling

the device with interface roughness. However, we also find that for devices with preferential doping configuration, these interference effects are minimized and a nearly ballistic behavior can be recovered.

2 Device structure and simulation

The device simulated here is a tri-gate n-MOSFET, built on an SOI wafer. Figure 1 shows a schematic of the device geometry we considered. The channel region is p-type and is left undoped. It is 10.8 nm long, 8.1 nm wide, and is surrounded by oxide on all sides, nominally 2 nm thick. The crystal orientation of the channel is chosen such that the current flows along the (100) direction. The source and drain regions are 18.47 nm wide and 9.8 nm long. The Si film is uniformly 6.51 nm high throughout the device. The source/drain regions are n-type doped with a nominal concentration of 10^{20} cm^{-3}. For a realistic treatment, following [5], a discrete dopant distribution has been considered.

In this study, we model the Si-SiO_2 interface roughness using an exponential auto-covariance function [6], with r.m.s. roughness 0.3 nm and correlation length 1.3 nm. Though these parameter values will depend upon the fabrication process, we assume that the surface can be characterized by parameters having values similar to the dry oxidation of (100) Si. SR scattering is included by using a non-uniform mesh, with mesh spacing down to 0.36 nm at the interface, close to the scale of an atomic layer (∼0.3 nm) [7]. This enables us to model the irregular nature of the interface without appreciably increasing the solution space. Figure 2 shows a vertical cross-section of the device to illustrate a typical interface generated using this scheme.

Theoretical simulation of the role of SR scattering in SNWTs has earlier been reported in [8] and for a DG-MOSFET in [9] using NEGF formalism. However, our 3-D recursive scattering matrix formalism based simulator [10], unlike the other two, is fully quantum mechanical in each direction, and all three directions are coupled. The 3-D Hamiltonian is defined for each slice of the device, and the transfer matrices which connect the adjacent slices are solved to get the propagating modes of the system. These transfer matrices are then cascaded, using a suitable numerically stable iterative procedure [11], to calculate transmission from source to drain. We also solve the system exactly even in the oversized source-drain regions, since in any practical device the source and the drain regions have external contacts, and therefore, are necessarily of larger area than the ultra-small channel. The modes excited in such an oversized source region will interact with the constriction present at the source-channel interface, and this should be considered when taking into account fully quantum mechanical transport.

3 Results and discussion

3.1 Effect of surface roughness

Figure 3 shows the I_D–V_G characteristics of the device for a representative set of simulations where the dopant distribution is kept identical. We simulate a device with no SR (• markers, dashed line in Fig. 3), and compare it to devices having different SR patterns. The r.m.s. roughness for these randomly different SR patterns is fixed at 0.3 nm. The drain bias V_D for all the simulations in this work is kept constant at 0.6 V.

SR causes some interesting quantum interference effects for large V_G values. For $V_G > V_T$, when the channel is populated with carriers, larger I_D values can be seen in devices that do not have a rough interface. The inclusion of SR causes

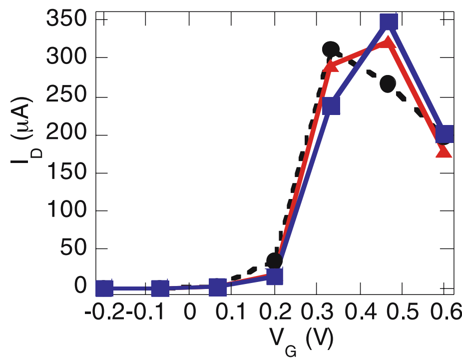

Fig. 3 I_D–V_G for a dopant distribution with moderate concentration of dopants near the critical source-channel interface

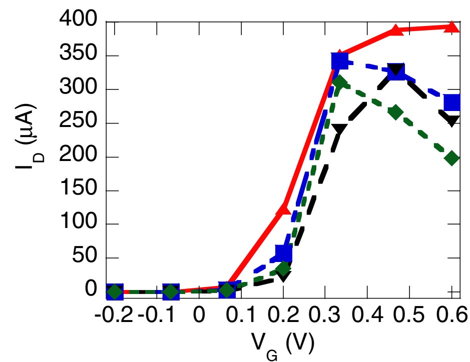

Fig. 4 I_D–V_G results for the SNWT for four random dopant distributions, neglecting SR. $V_D = 0.6$ V. Upper triangles (▲) denote the distribution which recovers nearly ballistic transport. Lower triangle (▼) represents the distribution which gives most degraded performance

a shift of the longitudinal states that are available for the carriers to tunnel through, from the source to the drain. Further, under constructive situations, this interference can result in an I_D value larger than in a 'smooth' device. (By 'smooth', we mean a device where SR is not considered.)

The devices with different SR patterns show similar characteristics. Below threshold, a reduction of I_D is observed, with an attendant increase of V_T. The subthreshold slope (SS) for these devices remains nearly constant, while the I_{on}/I_{off} ratio increases, indicating that SR scattering is more effective for carriers in the low field regime. This reduces I_{off} more than I_{on}, causing I_{on}/I_{off} to increase. The mean values of the operating parameters for the set of devices in this simulation are given in Table 1.

3.2 Effect of different dopant configurations

In Fig. 4 we show the I_D–V_G characteristics of the SNWT for four random distributions of the dopants in the source-drain regions, without considering SR. Though subthreshold behavior of the devices is similar, the linear plot shows considerable variation in I_D across these four devices. Fluctuations in I_D caused by the discrete dopants in the ultra-small channel region have been reported earlier [12–14]. However, these results show that such variations are unavoidable, even when the channel region is undoped and the dopants are confined to the source and drain regions. Experimental evidence of this fact is however, yet to be seen.

The positively charged dopants in the source and drain regions alter the potential profile experienced by the electrons, setting up points of interference. Stronger reflections are caused by dopants located close to the source-channel interface. Such a device turns on late (down triangles ▼, in Fig. 4). On the other hand, a device with few dopants close to the source-channel interface shows nearly ballistic behavior (up triangles ▲).

3.3 Effect of including SR with different dopant configurations

Next we include an identical SR pattern for the devices discussed in Section 3.2. In the subthreshold region, SR reduces I_D as the rough interface serves as an additional source of scattering. However, the large variation of I_D from the values of the 'smooth' devices at high V_G indicate that SR causes additional interference over and above the quantum interference induced by the dopant ions. This causes considerable spread in the device parameters (last row in Table 1). Below threshold, when the channel is not sufficiently populated, the rough interface cannot interfere effectively with the carrier density in the source region, and this explains the similar sub-threshold behavior across the devices. The deviation of I_D from that of the 'smooth' device is particularly large for the case where the shallow dopant ions also happen to be in close proximity to a rough section of the top gate-oxide-channel interface (▼ markers in Fig. 5). The carriers scattered from the interface get trapped in the potential field of the dopants in this case, thus aggravating the situation.

Table 1 Values of SNWT operating parameters for different simulations. Doping distribution for calculating parameters for rows 1 and 2 is kept identical to investigate the effect of various SR patterns

Parameters	V_T	ΔV_T	SS	ΔSS	I_{on}/I_{off}	$\Delta I_{on}/I_{off}$
Units	mV		mV/decade			
No SR.	99	–	67.71	–	897	–
Diff. SR.	144.9	2.5	68.79	0.39	1119	43.66
No SR. Diff. Dopant Dist.	93.1	9.53	68.08	2.28	692	107
Fixed SR. Diff. Dopant Dist.	127.5	19.1	70.33	2.43	741.4	145.24

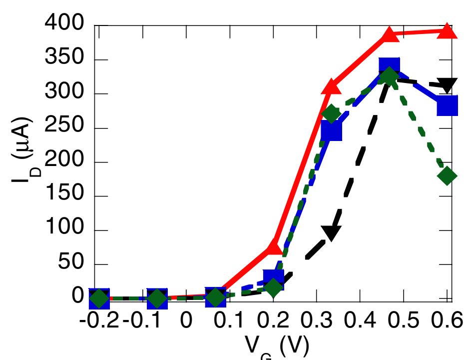

Fig. 5 I_D–V_G for the same dopant distributions as in Fig. 4, including SR. While one device (▲ markers) retains nearly ballistic behavior, there is a large deviation in I_D from the 'smooth' channel value for another device (▲ markers)

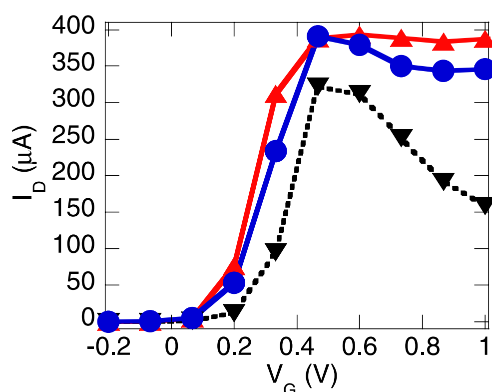

Fig. 6 I_D–V_G for three different dopant distributions, including (• – uniform distribution, ▲ – discrete distribution, with dopants away from the source-channel interface and ▼ – discrete distribution, with dopants located close to the source-channel interface), resulting in degraded I_D characteristics

The recovery of ballistic transport in a device which has comparatively fewer dopant ions located close to the source channel interface can be seen by comparing its I_D–V_G characteristics with that of a device having a uniform doping distribution, since in the latter device there is no quantum interference caused by discrete impurities. This comparison is shown in Fig. 6, where I_D–V_G plots, including SR scattering, is given for a set of three devices – a device with uniform dopant distribution (• markers), a device with few dopant ions close to the source-channel interface (▲ markers), and one with dopant ions close to the interface (▼ markers). The degradation of I_D in the device with more dopant ions located close to the source-channel interface is quite severe. This result clearly shows the improvement obtained by keeping dopant ions away from the critical source-channel interface.

4 Conclusion

A self-consistent 3-D fully quantum mechanical simulation of a silicon nanowire MOSFET has been made to investigate the effect of SR and discrete dopant distribution on device performance. SR increases scattering in the channel, causing a reduction of I_D below threshold, and an increase of V_T. For higher V_G, SR serves to modify the quantum interference of carriers with the discrete dopant ions, thereby setting up additional fluctuations in I_D, thus exacerbating device-to-device performance variation in terms of the operating parameters. However, it is heartening to find that if the dopant ions are located away from the source-channel interface, the current degradation is insignificant, and nearly ballistic behavior can be recovered. This underscores the importance of keeping dopants away from the critical source-channel interface and of maintaining a good quality oxide-silicon interface to achieve the best possible device performance.

References

1. Doyle, B. S. et al.: IEEE Elec Dev Lett. **24**, 263 (2003)
2. Marcyk, G.: Intel Terahertz Transistor releases, Sep. 17, 2002 Available: http://www.intel.com/technology/silicon/micron.htm
3. Yang, F.-L. et al.: VLSI Tech. Tech. Dig. 8 (2004)
4. Baie, X. et al.: Proc. IEEE Int. SOI Conf. 66 (1995)
5. Gilbert, M.J., Ferry, D.K.: Superlattices Microstruc. **34**, 277 (2003)
6. Goodnick, S.M. et al.: Phys. Rev. B **32**, 8171 (1985)
7. Brown, A.R. et al.: Superlattices and Microstruc. **34**, 283 (2003)
8. Wang, J. et al.: Appl. Phys. Lett. **87**, 043101 (2005)
9. Martinez, A. et al.: IEDM Tech. Dig. (2005)
10. Gilbert, M.J. and Ferry, D.K.: J. Appl. Phys. **95**, 7954 (2004)
11. Usuki, T. et al.: Phys. Rev. B, **52**, 8244 (1995)
12. Gilbert, M.J., Ferry, D.K.: IEEE Trans. Nanotechnology. **4**, 355 (2005)
13. Asenov, A.: Nanotechnology **10**, 153 (1999)
14. Brown, A.R. et al.: IEEE Trans. Nanotechnology **1**, 195 (2002)