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Full Quantum Mechanical Simulation of Ultra-Small Silicon Devices in Three-Dimensions: Physics and Issues

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Abstract. The combination of the need for alternative devices and the improvement in process technology has led to the examination of silicon quantum wires for future MOS technology. However, in order to properly model these devices, a full three-dimensional quantum mechanical treatment is required. In this paper, we present the results of a three-dimensional, fully quantum mechanical, self-consistent simulation of a silicon quantum wire MOSFET (Metal Oxide Field Effect Transistor) with a narrow channel (8 nm). A quasi-standing wave is formed in the narrow channel at certain gate voltages as the electron density is trapped in narrow channel. These effects are the result of two competing effects: (1) the interaction of the propagating electrons with the channel dopants, as well as with the dopants in the source and drain of the device. (2) the reflections from the boundaries that form the narrow channel both on the source side and the drain side.

Keywords: silicon on insulator, MOSFET, scattering matrices, 3D quantum simulation, quantum wire

1. Introduction

As traditional lithographic techniques are improved and new techniques are developed, the sizes of CMOS devices will continue to shrink. However, the traditional silicon MOSFET is proving to be inadequate for usage in new architectures. Therefore, other devices are currently under examination as possible candidates to replace the bulk MOSFET in future applications [1]. Of these possible replacements, one of the most interesting is the SOI (Silicon On Insulator) quantum wire MOSFET. It offers the advantages of SOI in that these quantum wire MOSFETs have an almost ideal subthreshold slope and improved DIBL as compared to bulk silicon devices. In addition to the operational benefits, the extremely small size of these wires makes them ideal for high packing density on wafers. Nevertheless, these devices present new challenges in terms of both the fabrication and the simulation. The relatively thin silicon film thicknesses associated with these devices ($\sim$5 nm) gives rise to quantization in the direction of the film growth. Recent experiments have shown that it is possible to fabricate MOS transistors in a SOI environment with channel *widths* as small as 2 nm [2]. This gives rise to quantization in the lateral direction, which cannot be separated from the other directions in the device. Therefore, as this push towards smaller devices continues, the need for an effective yet efficient simulation tool capable of describing the quantum mechanical nature of these devices in three dimensions is critical.

Recently, there has been work done on implementing a fully quantum mechanical three-dimensional Greenís functions approach to modeling the type of devices that we study in this paper [3]. While mathematically this approach may take care of the coupling of the excited modes through a unitary transformation, in order to obtain the two-dimensional electron subbands, it is still only fully quantum mechanical in one dimension. Moreover, the Green's functions naturally yield only the density of states, so that another difficult computation is required to find the density needed for closing the self-consistent loop. In this paper, we use a self-consistent variant of the scattering matrix formalism in

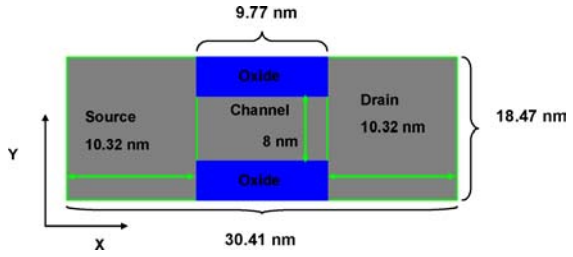

Figure 1. Schematic of device under consideration in the *xy* plane.

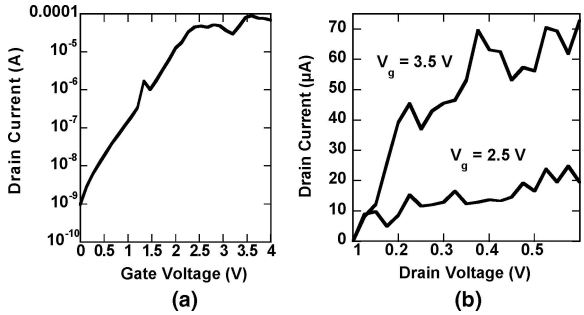

Figure 2. (a) $I_d - V_g$ curve for a quantum wire SOI MOSFET with a constant drain bias of 10 mV plotted on a logarithmic scale. (b) $I_d - V_d$ curves for a quantum wire SOI MOSFET.

three-dimensions which is fully quantum mechanical in each direction [4]. We apply this to a quantum wire MOSFET with a narrow channel of 8 nm. The use of this method gives us an advantage in the speed of the computation and removes the need to perform complicated integrations for the density as the latter is given naturally from our wave function amplitudes at each site.

2. Device Structure and Simulation Procedure

The device under consideration is a quantum wire SOI MOSFET, shown in Fig. 1. In general, we have a wide source and drain region which have doping concentrations of 1×10^{20} cm^{-3} *n*-type. The dimensions of the source and the drain are 18.47 nm wide, 10.32 nm long and 6.51 nm high (integer multiples of the Si atom spacing) corresponding to the thickness of the silicon layer. The channel of our device is a *p*-type region which has a doping concentration of 5×10^{18} cm^{-3}. In this device, the channel region is 8 nm wide, 9.77 nm long and 6.51 nm high. In these simulations, we have used exact device dimensions, in terms of the silicon lattice parameter, to ease the inclusion of discrete dopants in the program. The source and drain of this device have an exaggerated size to exacerbate the interaction of the modes excited in the source with the constriction present at the source-channel interface. It should be noted that, on either side of the narrow channel, we have included oxide regions to confine the density rather than impose hard wall boundary conditions.

3. Device Results

In Fig. 2(a) we plot an $I_d - V_g$ curve on a logarithmic scale for the case of a drain bias of 100 mV. From this figure, it is easy to see that quantum interference is produced by the dopants present in the device, and this has a profound effect on the output current. At certain gate biases, the output currents may have spikes as much as several orders of magnitude larger than the background current. These spikes correspond to the incident electron wave tunneling through resonant states formed in the channel a quasi-corral of positive channel acceptor potentials. Naturally, this phenomenon depends strongly on the positions of the acceptors in the channel. In the case of this device, the channel dopants are placed almost equidistant from each other at the center of the channel and at approximately the same height. This placement maximizes the interference effects. In Fig. 2(b), we plot the $I_d - V_d$ curves. These curves exhibit a basic transistor behavior with current saturation, but peaks in the current are still present even at elevated voltages. This is due to the integration over highly transmitting states that are present in the system. The peaks in transmission are present at many different energies and thus we should expect to see the peaks in the output currents at higher energies.

In Fig. 3, we examine the electron density at a depth of 3 nm into the silicon layer at a gate voltage of 0 V. For each of the electron density plots presented, we examine only the source driven electron density (as in classical MOSFETs, the current can be separated into a source-derived part and a drain-derived part). Self-consistency cannot be achieved without both sources of electron density, but the use of the positive propagating electron density shows better how the electrons interact with the channel dopants and how they occupy the preferential states formed in the source and the drain of the device. In Fig. 3, the black dots are the dopants. The relative size of each dopant spot shows how deep they are in the silicon layer. Dopants that are closer to the surface of the device have a larger spot, while those that are deeper in the device are smaller. The

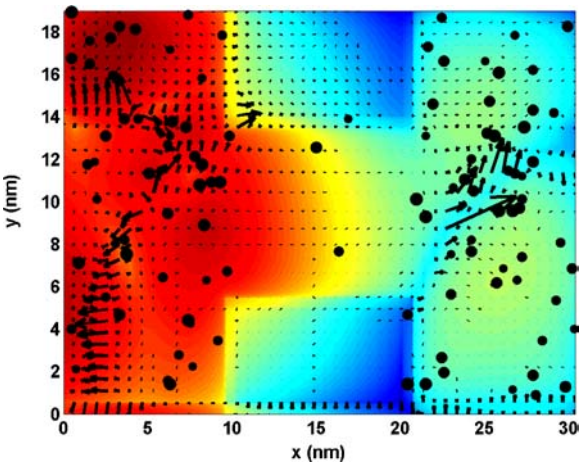

Figure 3. Electron density 3 nm into the silicon layer at $V_g = 0$ V.

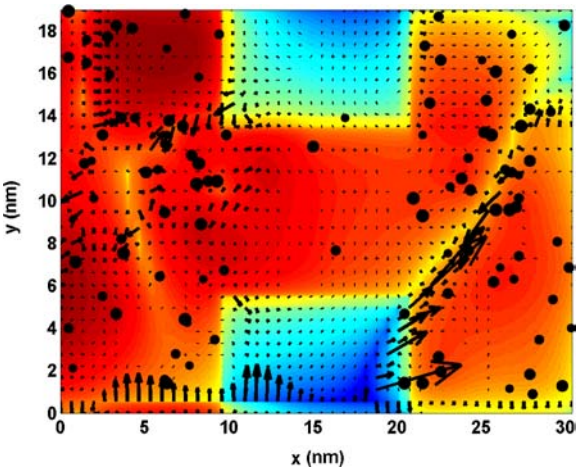

Figure 4. Electron density 3 nm into the silicon layer at $V_g = 1.667$ V.

arrows present on the figure correspond to the velocity field for both positive and negative flowing states. The size of the arrows corresponds to the velocity field at that point with large arrows corresponding to large velocities. We compute the velocity field by writing the wavefunction as,

$$\psi = Re^{i\frac{S}{\hbar}} \tag{1}$$

where S and R are real. The velocity field may then be computed by

$$\frac{dr}{dt} = \frac{\nabla S}{m} = \frac{\hbar}{m}\mathrm{lm}(\nabla \ln \psi) \tag{2}$$

Figure 3 clearly shows the effects of a self-consistent solution. We see that the density present in the source and drain sits on the sites near the dopants at that depth. Had the solution not been self-consistent, the density would tend to sit in blobs corresponding to the shape of the modes. As mentioned, the electron density plotted in all of the following figures is the source-derived density. While both positive and negative propagating densities were used in the self-consistent process, only the positive density is plotted here.

In Fig. 4, we plot the electron density for a gate voltage of 1.67 V and a drain bias of 10 mV. This gate voltage is close to the threshold voltage of the device as is evidenced by the increased electron presence in the channel. (In these simulations, we have made no adjustments for flat-band shifts arising from work-function differences. In a final simulation, the gate work function would be properly chosen to adjust the threshold voltage to a more desirable point for lower bias values.) We also see an increased presence of electrons sitting in the preferential sites in the drain. While all of this is to be expected in a device that is biased close to threshold, the most interesting aspect of Fig. 4 is the interaction of the electrons with the channel dopants. We can clearly see that the electron density piles up on the source side of the channel and then is forced to navigate through the center of the dopants as the electrons lack sufficient energy to move to either side of the dopant. It is this interaction that causes the resonances in the output currents.

In Fig. 5, the gate voltage is further increased to 1.8 V. The device is now very close to threshold and

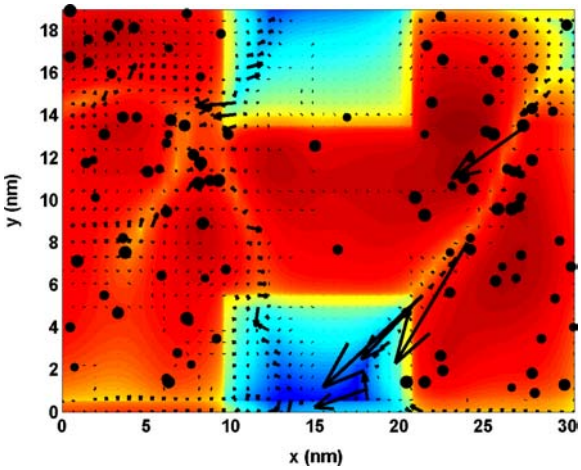

Figure 5. Electron density taken at a depth of 3 nm into the silicon layer at $V_g = 1.800$ V.

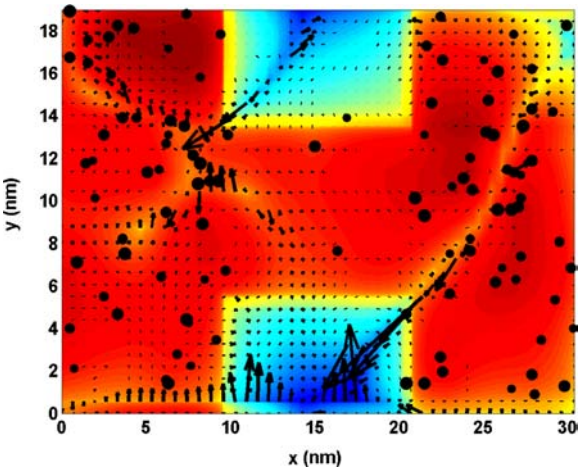

Figure 6. Electron density taken at a depth of 3 nm into the silicon layer at $V_g = 1.933$ V.

the electron density can still be seen filtering through the channel dopants. At this point, the available states in the channel are completely filled. A standing wave is formed in the channel of the device. This is apparent from the fact that there are no high velocities in the channel of the device. As the density enters the channel, the majority of the density in the source is reflected at the interface. Once in the channel the density then undergoes a second reflection as it attempts to leave the channel. Typically in these devices the lack of channel velocities show that the reflections from the source-channel interface and the channel-drain interface are beginning to set up a standing wave in the channel of the device. However, this is not the only reflection in the channel. The density must also navigate through the channel dopants as it attempts to form the standing wave, but this effect is small in comparison to the reflections from the channel ends. The main effect of the channel dopants is to reroute the paths of the carriers and to reduce the velocities. We do notice that there are some velocities on the source side of the channel as the density prepares to depopulate with the next increase in the gate voltage.

In Fig. 6, we raise the gate voltage to 1.93 V. Here, the density that had begun to fill the channel in Fig. 5 has now started to leave the channel. This depopulation is evidenced by the larger velocities present on the source side of the channel. Electrons that are currently populating the channel states are moving into the available drain states as more electrons enter the channel.

4. Conclusions

We have presented results of a quantum wire SOI MOSFET with a narrow channel region. The interaction of the electrons with the channel dopants causes peaks in the output current due to the formation of additional channel levels for the electrons to tunnel through. We have also seen that the electron density will form standing waves in the channel of the device at certain gate voltages. This is due mainly to the fact that, as the density tunnels into the channel and then attempts to leave, it undergoes a series of reflections at the interfaces. These reflections trap the density in the channel.

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