Indium arsenide quantum wire trigate metal oxide semiconductor field effect transistor

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We present the results of a three-dimensional, self-consistent ballistic quantum mechanical simulation of an indium arsenide (InAs) quantum wire metal oxide semiconductor field effect transistor with channel lengths of 30 and 10 nm. We find that both devices exhibit exceptional I_{on}/I_{off} ratio, reasonable subthreshold swing, and reduced threshold voltage variation. Furthermore, we find that the current in the 30 nm case is reduced at the high voltage end of the gate sweep due in part to interference due to lateral states set up in the channel of the device, but in the shorter channel case we do not find this effect for the voltages swept. This effect can be easily seen in the electron density as the perturbations in the density. We also find these states present in the drain voltage sweeps as well. These states present a possible problem for use in complementary metal oxide semiconductor architectures. Finally, we compare the performance of the 10 nm InAs trigate device to a similar silicon device. We find that, when a suitable gate material and doping density is chosen, the InAs devices perform comparably to silicon devices in the ballistic limit. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2179135]

I. INTRODUCTION

It has been a well established fact that the semiconductor industry must devise an alternative solution to the bulk silicon metal oxide semiconductor field effect transistor (MOSFET) in order to continue the relentless scaling of device density. One of the most promising of these technologies is the quantum wire MOSFET. Trigate devices offer greatly improved electrostatic control over the channel of the device when compared to the traditional MOSFET due to the presence of the additional gates.[1] With a device of this nature, it is necessary to use a simulation tool that takes into account the quantum confinement in the system. Previously, one only had confinement in the direction perpendicular to the gate, but the width of the channel is now on the order of the Fermi wavelength of the electron. There have been many different simulations of the ballistic operation of these devices.[2,3]

Within the last few years, there has been a renewed interest in the use of III-V materials instead of silicon for future generation transistors. Previous studies have shown that care must be taken in the fabrication of these devices or large increases in the output drain current (kink effect) occur.[4,5] Through the use of quantum wires with discrete subbands for the active regions of the device, the kink effect may be eliminated. Nevertheless, there has been interest in MOSFETs in these III-V materials for use in high speed logic applications.[6]

In this paper, we present the results of a three-dimensional, self-consistent, quantum mechanical device simulation of a trigate InAs quantum wire MOSFET with discrete dopants included as the only scattering mechanism (impurity scattering). We examine some of the pertinent device characteristics and functional parameters surrounding the operation of devices with 30 and 10 nm channel lengths. We then make a comparison between the performance of 10 nm InAs and silicon devices.

II. METHOD AND DEVICE STRUCTURE

In Fig. 1, we display a schematic of the device geometry for an InAs MOSFET with a 30 nm channel taken to lie in the *x*-*y* plane (the *z* axis is normal to the plane shown). The exact device dimensions (multiples of the lattice constant) have been included in this simulation to aid in the inclusion of the discrete dopants. The thickness of the InAs layer is 9.09 nm. The source and drain of the device are *n* type with a doping density of 6×10^{18} cm^{-3}, while the channel of the device is considered to be *p* type but undoped. The gate material is assumed to be platinum and the gate oxide on each side is composed of 1 nm of hafnium oxide (HfO_2). Underneath the device, we have assumed a generic insulating substrate. The structure of the device with the 9.69 nm channel is exactly the same with the exception, of course, of the channel length. Once the device geometry is defined, the InAs lattice is scanned and the dopants are distributed ac-

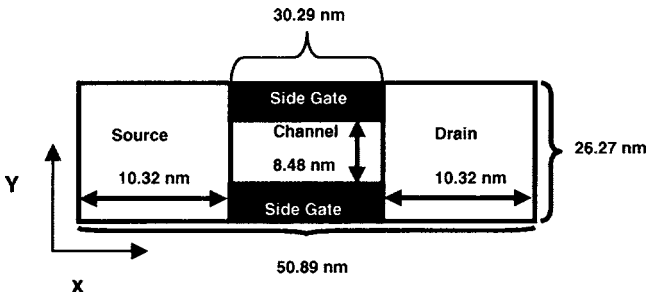

FIG. 1. Device structure in the *x*-*y* plane for the 30 nm device.

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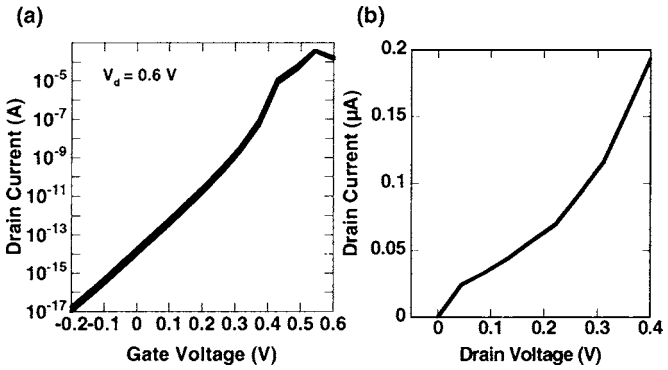

FIG. 2. (a) I_d-V_g curves for two different 30 nm devices. (b) I_d-V_d curve for a 30 nm device with V_g=0.4 V.

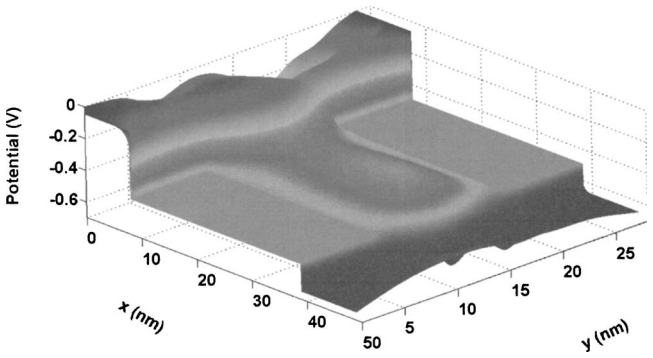

FIG. 3. Device potential in the x-y plane taken at a depth of 7 nm into the device at V_g=0.43 V and V_d=0.6 V.

cording to the method presented in Ref. 7. Following the distribution of the dopants, they are then mapped back onto the grid of the simulation mesh and the initial self-consistent Poisson solution is obtained. In this case, the full Coulomb potential of the dopants is incorporated. Then, the solution of Poisson's equation for the local potential is no longer smoothly varying in the source and the drain of the device. The inclusion of discrete dopants causes the formation of potential variation in the source and drain. The density throughout the device is calculated using a variant of the recursive scattering matrix method which solves the Schrödinger equation in the effective mass approximation as described in Ref. 2. In short, this method provides us with a three-dimensional, fully quantum mechanical method. Since the transport calculation is performed in real space, the different excited modes in the system are automatically coupled unlike in other simulations.[3] In order to achieve self-consistency, the density obtained from the transport calculation is then updated using Broyden's method[8] and a guess for the potential is obtained through the solution of Poisson's equation. The process is repeated until a desired level of convergence is obtained. It should be noted that all of the simulations presented here have been performed at 300 K and impurity scattering is the only scattering mechanism considered. Furthermore, we also only consider transport in the gamma valley. Upper valley transport and scattering will be considered in future work.

III. RESULTS

A. 30 nm device

In Fig. 2, we plot the I_d-V_g and I_d-V_d curves for the 30 nm InAs quantum wire MOSFET. We find that the subthreshold slope averages about 69 mV/dec and the threshold voltage is 0.46±0.02 V. The I_{on}/I_{off} ratio is 1.9×10^{10}. These numbers predict a transistor whose currents and charge control should far exceed those of its silicon counterpart. However, the threshold voltage for the devices is too large to be used in the present or the next generation technologies. This is due to the fact that, in an InAs system, we have large quantization effects and gate work function dependence. This has both good and bad aspects. First, one normally expects InAs to have a Fermi level pinned roughly 0.4 eV into the conduction band. But, MOS operation has long been known to occur in this system.[9] Thus, a proper choice of the metal gate is essential to selecting the proper threshold voltage. We have not optimized this process in this report, but quantization in the channel helps to move the Fermi level out of the conduction band. However, in the present simulation, larger voltages must be applied to the system for conduction to occur. While the threshold voltage is too high in this system, the amount that the threshold voltage varies from device to device is minimal. From Fig. 2(a), two I_d-V_g curves are compared and these lie almost on top of one another. This invariance to threshold voltage shifts lies in the fact that we do not need to dope these devices to as high a concentration as is required in silicon.

With fewer dopants in the source and drain of the device, there is a greatly reduced electron interaction with these dopants resulting in smaller shifts. Another interesting point found in Fig. 2(a) is the sharp decrease in the output currents found at V_g=0.6 V. This is due to competing effects between the multiple scattering events undergone by the incident electrons[10] and interference from longitudinal states in the channel of the device.[11] These effects are best seen in the electron density, which will be discussed below. Nevertheless, we can see that it would be advantageous to operate this device at voltages smaller than when this interference and scattering becomes appreciable for best reliability. In Fig. 2(b), we show the I_d-V_d curve for the 30 nm device with a gate voltage of 0.4 V applied. Here we see a clear downside to the InAs transistor in that the drain voltage never reaches saturation. This is an effect that can be attributed to the comparably small band gap of InAs. Initially, we see that at low drain voltages (<0.15 V) the curve behaves rather normally, but as the drain voltage is increased we find that the current does not saturate. This is due to the fact that the drain voltage does not effectively pinch off the channel. In Fig. 3, we plot the potential at a depth of 7 nm into the device with a gate voltage of V_g=0.43 V and V_d=0.6 V. Here we observe that near the drain end of the device there is no appreciable drop in the potential that would normally be associated with the pinch-off condition observed in many MOSFET devices. We can further rule out the effects of impact ionization in these devices due to the quantization present in the system and the fact that this process is not included within the physics of the present simulation.

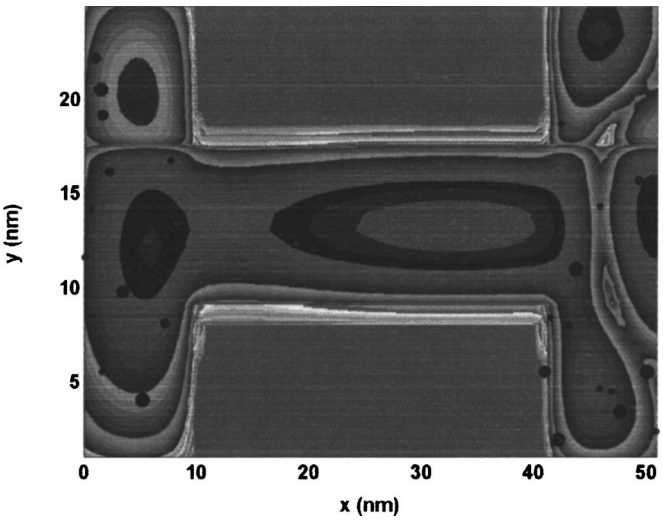

FIG. 4. Electron density in the x-y plane taken at a depth of 7 nm into the device at V_g=0.43 V.

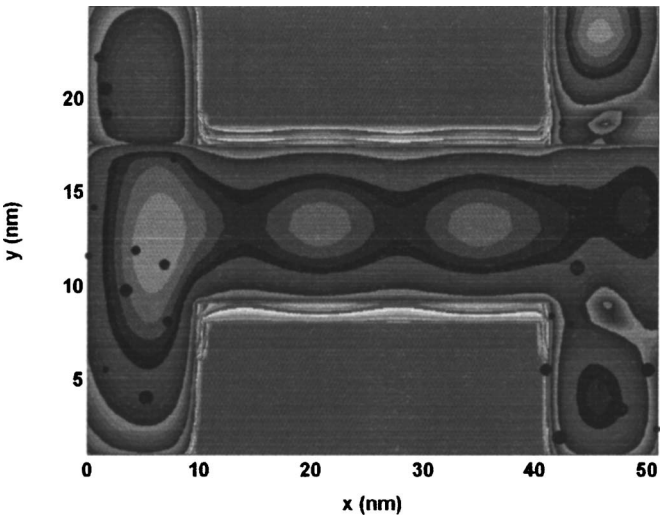

FIG. 6. Electron density in the x-y plane taken at a depth of 7 nm into the device at V_g=0.6 V. We see clear perturbations in the channel electron density due to tunneling.

In Fig. 4, we plot the electron density in the x-y plane taken at a depth of 7 nm into the device. The black dots in the figure represent the locations of the dopant atoms in the system. Dots that are larger in size are closer to the surface of the device, while dots that are smaller are buried farther down in the device. Here we plot the density at V_g=0.43 V. At this voltage, we are clearly above the threshold voltage for the device. The channel is now fully populated with carriers. In the source and drain, the location of the electron density depends rather weakly on the locations of the dopants. This is mainly due to the scarcity of the dopants. With the channel so populated, we know that we are close to the maximum output current for this device. The placement of the density is better explained through the use of Fig. 3. Here we see the potential barriers in the source and drain of the 30 nm device preventing the spread of electrons across these regions. Further, we also see that there is a potential barrier at the end of the channel of the device. In Fig. 5, we plot the one-dimensional potential passing through the middle of the device at a depth of 7 nm. Here, we may clearly determine that the height of this potential barrier is approximately $2.1k_bT$ corresponding to the discrepancy in the channel electron density, from beginning to end, of about two orders of magnitude. The presence of the barrier has now caused the incident electron density to undergo an additional reflection off the barrier at the end of the channel forming the depression in density at the beginning of the channel, while the remainder of the density tunnels through the barrier to reach the drain. Furthermore, we also notice that the drain potential does not resemble a device that is in the pinch-off regime. The nonzero value of the electron density at the drain end of the device is responsible for the behavior seen in Fig. 2(b).

This figure is to now be contrasted with Fig. 6 in which we plot the electron density at the same depth in the device but with V_g=0.6 V. We find that the channel is slightly more populated at V_g=0.6 V than at V_g=0.43 V. This is due to source-drain interferences with the resultant formation of tunneling barriers. The more interesting detail is the fact that these perturbations in the electron density due to the barriers can be seen. In Fig. 7, we plot the potential at a depth of 7 nm into the device at a gate voltage of V_g=0.6 V and a drain voltage of V_d=0.6 V. Here we see that the barrier

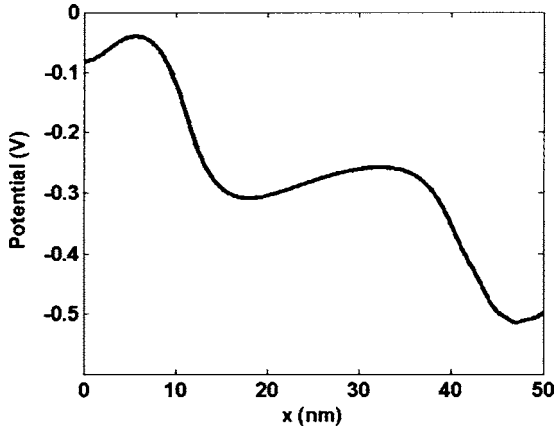

FIG. 5. One-dimensional potential plot taken through the center of the channel of a 30 nm InAs quantum wire transistor at a depth of 7 nm at V_g =0.43 V and V_d=0.6 V.

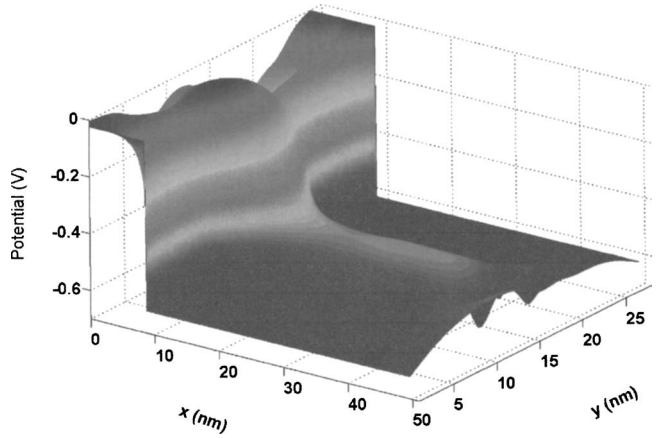

FIG. 7. Device potential in the x-y plane taken at a depth of 7 nm into the device at V_g=0.6 V and V_d=0.6 V.

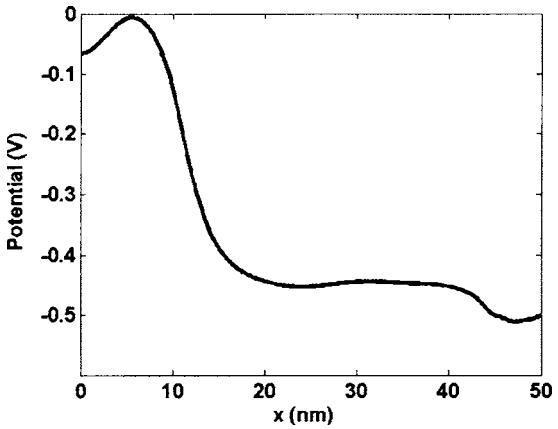

FIG. 8. One-dimensional potential plot taken through the center of the channel of a 30 nm InAs quantum wire transistor at a depth of 7 nm at V_g =0.6 V and V_d=0.6 V.

present at the drain end of the channel has been greatly reduced. Now we see that the once omnipresent tunnel barrier has now become several smaller tunnel barriers that cause the density to undergo multiple reflections in the channel giving the density its final form as seen in Fig. 6. The multiple reflections cause the reduction in channel transmission which causes the reduced output current at this elevated gate voltage. In Fig. 8, we plot the one-dimensional potential through the center of the device again at a depth of 7 nm. We confirm the reduction of the potential barrier and find the peak to trough ratio of the barriers in the channel to be $0.46k_bT$ corresponding to an electron density discrepancy between the peaks in Fig. 6 of less than one order of magnitude. Again, we notice that the potential does not resemble that of a device that has reached pinch off despite the long channel length.

B. 10 nm device

In Fig. 9, we plot the I_d-V_g and I_d-V_d curves for the 10 nm InAs quantum wire MOSFET. The subthreshold slope averages 169 mV/dec and the threshold voltage is 0.41 ± 0.04 V. The I_{on}/I_{off} ratio is 4×10^3. Even at a gate length of 10 nm, we still find that these InAs devices perform well. The degraded subthreshold slope that is found in the 10 nm device is due to the increased effect of the gate

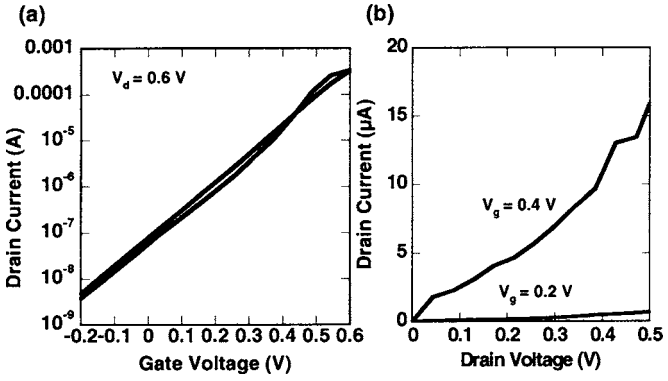

FIG. 9. (a) I_d-V_g curves for two different 10 nm devices. (b) I_d-V_d curves for a 10 nm device.

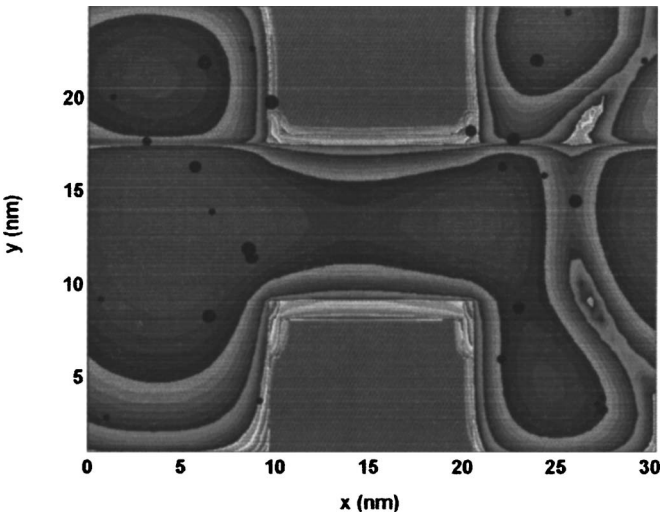

FIG. 10. Electron density in the x-y plane taken at a depth of 7 nm into the 10 nm device at V_g=0.43 V.

work function, enhanced source-to-drain tunneling and quantization, and a larger separation between successive subbands, as compared to similar silicon devices, found in these InAs devices. Large changes in the channel field produce smaller changes in the current than in the 30 nm case. In Fig. 9(a), we find that the I_d-V_g curves for these devices appear more standard when compared to the 30 nm case. Yet, we are capable of applying quite large voltages without the longitudinal states affecting the output current. When we examine the I_d-V_d curves in Fig. 9(b), we see the same general behavior as that in Fig. 2(b); there are some additional interference effects in the V_g=0.4 V curve when the drain voltage exceeds 0.4 V.

In Fig. 10, we plot the electron density for the 10 nm InAs quantum wire device at V_g=0.43 V. As in Fig. 4, we find that the channel is now fully populated. As the density exits the channel of the device, we see that the density begins to populate some of the preferential sites in the drain. This is a self-consistent effect, as without the self-consistency, the density would simply pool into blobs roughly the shape of the modes. Interestingly, we see that the channel densities seem rather smooth when compared to the densities seen in the 30 nm case. In Fig. 11, we plot the electron density in the 10 nm device for V_g=0.6 V. Here we begin to see signs of the perturbations due to the tunnel barriers as seen in Fig. 6 for the 30 nm device. We observe a null in the electron density towards the drain side of the channel. This depression in electron density has formed from the interaction of the incident and channel-drain reflected waves and the interaction with the tunnel barriers but does not produce a significant drop in current. In Fig. 12, we plot the potential at a depth of 7 nm into the device corresponding to a gate voltage of V_g =0.6 V and drain voltage of V_d=0.6 V. We find that while the channel tunnel barriers are not present in the 10 nm case, we do find a $1.75k_bT$ barrier near the channel-drain interface. It is this barrier that causes the drain to be only slightly more populated in Fig. 11 than that in Fig. 10. In addition to the barrier being responsible for the minimal drain density increase, it is responsible for the drop in electron density at the

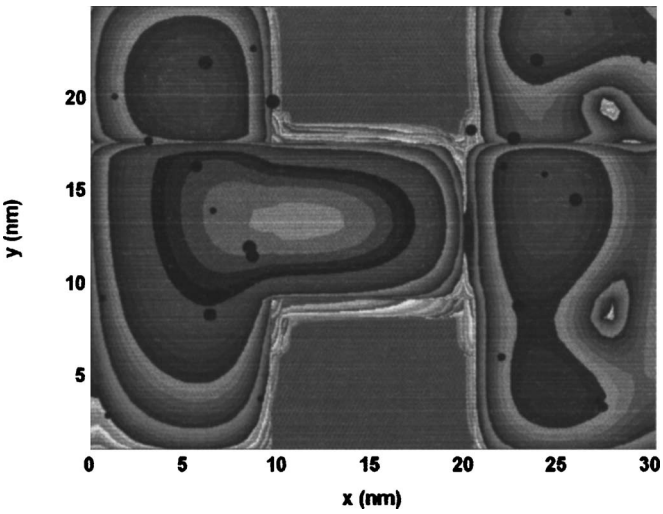

FIG. 11. Electron density in the x-y plane taken at a depth of 7 nm into the device at V_g=0.6 V. There are no perturbations in the channel electron density due to tunneling as were present in the 30 nm case.

end of the channel and the charge pileup at the beginning of the channel. In Fig. 13, we plot the one-dimensional potential through the center of the channel at a depth of 7 nm. We find that the presence of a dopant ion in the drain in series with the rising potential barrier results in the form of the electron density observed in Fig. 11. However, we also note that there is no evidence of pinch off in this plot which validates our conclusions for the behavior in Fig. 9(b).

C. Comparison to silicon quantum wire trigate MOSFET

Now that the basic performance characteristics for the InAs devices have been outlined, the question that begs to be addressed is the question of how these devices perform when compared to silicon counterparts. Therefore, we wish to compare the operation of two 10 nm devices, one in a silicon quantum wire and one device in InAs, of the exact same geometry as used to obtain the previous results. Nevertheless, some small modifications have to be made to the silicon device to account for the material differences. In the silicon quantum wire trigate MOSFET, we use a silicon thickness of 6.51 nm and the length of the channel is set to be 9.77 nm. To account for the differences in thicknesses and lengths, we

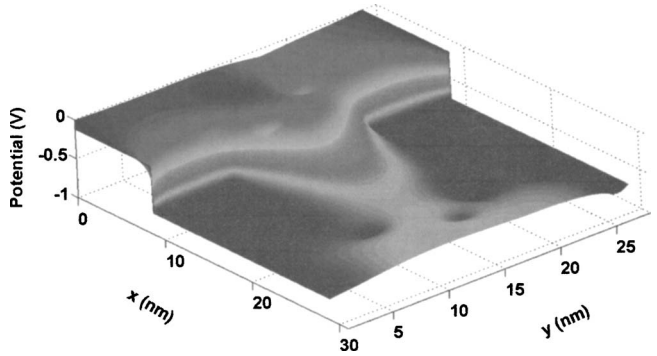

FIG. 12. Device potential for 10 nm InAs trigate quantum wire device in the x-y plane taken at a depth of 7 nm into the device at V_g=0.6 V and V_d=0.6 V.

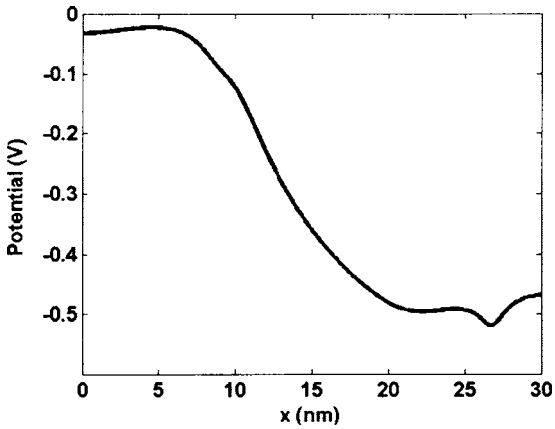

FIG. 13. One-dimensional potential plot taken through the center of the channel of a 10 nm InAs quantum wire transistor at a depth of 7 nm at V_g=0.6 V and V_d=0.6 V.

adjust the doping of the silicon device in the source and drain to 1×10^{20} cm^{-3}, while the channel of the device is again left undoped. With these adjustments we find that we have an identical number of subbands occupied in the source and drain of both the silicon and InAs devices. Yet, we must deal with one additional issue before the devices can be compared, and this is the issue of the threshold voltage. For a device to be considered for use in future complementary metal oxide semiconductor (CMOS) applications, we typically desire a threshold voltage of around 0.2 V. Clearly, by examining Fig. 9, we find that the threshold voltage for the InAs devices is far too high. In order to lower the threshold voltage, we have several mechanisms at our disposal. First, we can decrease the length of the channel which would have the effect of decreasing the source-channel barrier which would allow greater transmission of states at lower gate voltages, thereby increasing the current. However, decreasing the length of an already nanoscale channel would require more complicated lithography and would increase the overall device leakage.

A second option for reducing the threshold voltage is to increase the source-drain doping. This would raise the Fermi level in the source, increasing the energies of the carriers in the source of the device. These more energetic carriers would then have greater transmissions through the source-channel barrier giving rise to an increased current. The disadvantages of increasing the doping in the device lies in the effect of introducing more device-to-device variation as we essentially would increase the electron-impurity interaction leading to quantum interference effects that scale with the number of dopants in the source and drain. These quantum interference effects then cause the statistical deviations in key parameters, as seen in previous sections.

Perhaps a better option than the two previously presented is to use different gate work function engineering. This is a desirable option as we can adjust the threshold voltage without introducing additional scattering or creating further lithographical complications. The previous simulations were carried out using a generic metal that had a work function of φ_{ms}=5.5 eV which roughly corresponds to that

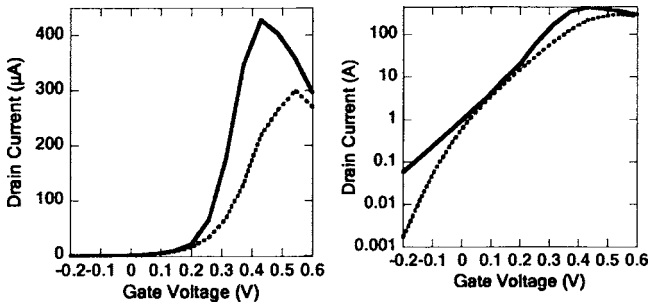

FIG. 14. I_d-V_g curve for InAs (solid) and silicon (dashed) quantum wire trigate transistors.

of platinum. Therefore, we replace the platinum contact with a titanium nitride contact with a work function of φ_{ms} =5.3 eV.

In Fig. 14, we plot the I_d-V_g curves for the 10 nm InAs and Si quantum wire MOSFETs. With the titanium nitride contact replacing the previous platinum contact, we now find that the threshold voltage for the device has shifted to 0.23 ± 0.04 V which is a significant improvement over the 0.41 ± 0.04 V we observed earlier. The variation of the threshold voltage remains constant when the platinum contact is switched for the titanium nitride contact due to the fact that we have not changed the doping in the source and drain of the device. The subthreshold slope of the device averages to be 163.05 mV/dec and the I_{on}/I_{off} ratio is about 700. For the silicon device, we find that the threshold voltage for six devices averages to be 0.26 ± 0.12 V with an average subthreshold swing of 66.53 mV/dec. The I_{on}/I_{off} ratio averages to be about 900. Based on these data, we conclude that the InAs device is, at best, only marginally competitive with a comparable silicon based device. We find that even with the gate material adjustment, the I_{on}/I_{off} ratio fails to approach the value we find in the 30 nm devices. Furthermore, by changing the gate material, we find that now the longitudinal states in the channel begin to show up in the output characteristics. This was not the case in Fig. 9, where the effects of the longitudinal states were suppressed.

In Fig. 15, we plot the I_d-V_d curves for the 10 nm InAs and Si quantum wire MOSFETs corresponding to gate voltages of (a) V_g=0.2 V and (b) V_g=0.4 V. In Fig. 11(a), we observe that the silicon I_d-V_d curve actually produces more subthreshold current under the identical bias conditions than

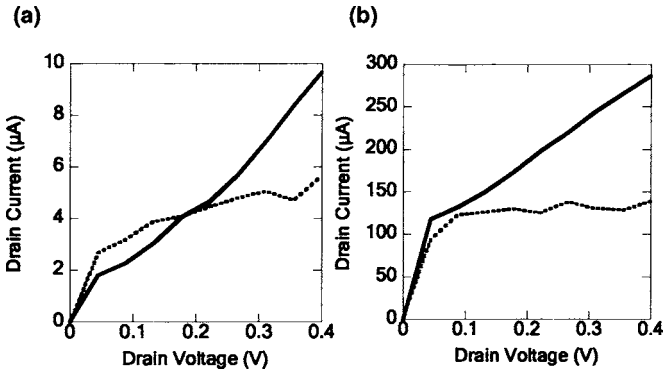

FIG. 15. I_d-V_d curves for InAs (solid) and silicon (dashed) quantum wire trigate transistors with (a) V_g=0.2 V and (b) V_g=0.4 V.

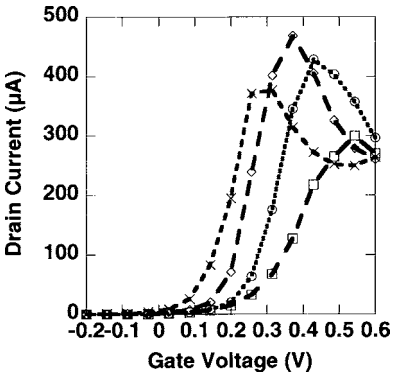

FIG. 16. I_d-V_g curves for 10 nm InAs devices with source and drain dopings of 6×10^{18} cm^{-3} (circle), 7×10^{18} cm^{-3} (diamond), and 8×10^{18} cm^{-3} (cross) and modified gate stacks with a 10 nm silicon quantum wire MOSFET with source and drain doping of 1×10^{20} cm^{-3} (square).

the InAs device. This arises from the fact that the InAs device suffers from a degraded subthreshold slope. Furthermore, we find that the InAs device does not saturate as the silicon device does. This eventually causes the output current in the InAs device, at high drain voltages, to exceed that of the silicon device. This behavior is attributed to the inability of the drain to effectively pinch off the channel of the InAs devices. In Fig. 15(b), we find that the I_d-V_d curves for the InAs device now outperform the silicon device at both low and high drain bias. While the device performance is better than that of the V_g=0.2 V case, we still find that the output currents suffer from the band gap tunneling which causes the device currents to fail to saturate as in silicon. We expect that this effect should be somewhat quenched when phonon and roughness scatterings are considered. As expected, in both the V_g=0.2 V and V_g=0.4 V cases, we see almost no evidence of quantum interference effects. Once again, this is due to the significant reduction of dopants present in the system. With reduced scattering, only the interactions with the boundaries will produce interference and this interaction is of less importance to device performance than the dopant-electron interactions.

While at this point, it is clear that the use of InAs devices provide some significant advantages over the use of silicon, we have seen in Fig. 15(a) that in the low bias regime, the silicon device can still outperform the InAs device. We now examine the effect of adding small increases to the source and drain doping. This will have the effect of reducing the threshold voltage, but the addition of more dopants could possibly cause additional unwanted interference effects to manifest themselves. Furthermore, the additional dopants will also increase the output currents which should increase the performance. To examine this assertion, in Fig. 16, we plot the I_d-V_g curves corresponding to InAs source and drain dopings of 6×10^{18}, 7×10^{18}, and 8×10^{18} cm^{-3} and modified gate stacks, with a silicon quantum wire MOSFET with source and drain doping of 1×10^{20} cm^{-3}. Once again the channel lengths of the quantum wire devices under consideration here are both approximately 10 nm. For the InAs device with a source-drain doping of 7×10^{18} cm^{-3}, we find that the threshold voltage is 0.172 V, the subthreshold swing is 83 mV/dec, and the I_{on}/I_{off} ratio is 200. When the doping

is increased to 8×10^{18} cm^{-3}, we find that the threshold voltage is 0.06 V, the subthreshold swing is 82 mV/dec, and the I_{on}/I_{off} ratio is 66. These results show that, by the simple addition of four dopant atoms, the threshold voltage can be reduced by almost 0.3 V, which is impossible in silicon. This could potentially present quite a problem as it is clear that unintentional doping would have a dramatic effect on device operation. Unfortunately, while the threshold voltage is exceptionally sensitive to the device doping, so is the I_{on}/I_{off} ratio. We find that the I_{on}/I_{off} ratio decreases significantly when the device doping is increased. This is due to the tunneling of electrons through the source-channel barrier as a result of an increased Fermi energy. Further, while the effects of interference and the formation of tunneling barriers can be seen in each of the curves, it has a more pronounced effect on the InAs device doped to 8×10^{18} cm^{-3}. Due to the increased source electron energy, the electrons begin to tunnel through longitudinal barriers and the current begins to oscillate in each of the curves. This effect happens well within the operational voltage range for this device, and this would lead to very hard voltage constraints in eventual circuit implementations. Moreover, we find that these devices still do not outperform the silicon device. The silicon quantum wire MOSFET has better subthreshold slope and I_{on}/I_{off} ratio and, through the use of either gate stack modifications or doping enhancement, the threshold voltage can be brought down to a reasonable level.

IV. CONCLUSIONS

In this paper, we have presented the results of three-dimensional, self-consistent ballistic transport simulations of InAs trigate quantum wire MOSFETs with varying channel lengths, doping densities, and gate materials and compare the performance of a 10 nm InAs device to that of a comparable silicon device. We find that, for a channel length of 30 nm, the InAs device provides excellent characteristics for use as a logic transistor. It has an almost ideal subthreshold slope and outstanding I_{on}/I_{off} ratio which varies over ten orders of magnitude, but under drain voltage sweeps, the current never truly saturates due to narrow band gap effects. The operation of the 10 nm device is, in many respects, much improved over that of silicon with the exception of a relatively high threshold voltage and subthreshold slope. These effects are attributed to the effect of the gate metal, the large subband separation in InAs, and tunneling effects. When the gate metal is switched from the generic contact to that of titanium nitride, we find that the threshold voltage is shifted by almost 0.2 V thereby making it similar to that of the silicon device. However, the subthreshold slope and I_{on}/I_{off} ratio for the device make it competitive with silicon, at best. In addition, we find that the I_d-V_d curves for the 10 nm InAs device suffer from significant quantum interference effects and poor current saturation. Finally, we study the effect of increased doping on the 10 nm devices. As the doping is increased, the threshold voltage decreases along with the I_{on}/I_{off} ratio. We conclude that, for longer length channels, the InAs device will outperform the silicon equivalent, but at reduced channel lengths, the silicon device offers better performance in the ballistic regime.

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