Some Considerations on Nanowires in Nanoelectronics

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(Invited Paper)

***Abstract*—Nanowires have become of great interest in recent years, and great promise has followed their development. In this paper, we review the role of ballistic transport, the ballistic-to-diffusive crossover, and the possible impact of nanowires in integrated circuits.**

***Index Terms*—Ballistic transport, field-effect transistors, nanowires, semiconductor transport.**

I. Introduction

RESEARCH on the growth and utilization of semiconductor nanowires has blossomed over the past few years [1], [2]. Nanowires have been extensively pursued for the creation of very small semiconductor field-effect transistors and have been predicted to be the solution to many ills as we approach the end of the roadmap and Moore's Law [3]. In these device studies, the nanowires are usually placed horizontal on an oxidized Si surface, and then, source and drain contacts evaporated to create the device. Here, the back Si is used as the gate electrode. While making a primitive device, it has not stopped various authors from claiming fantastic performance from such devices, which is a result not usually found by more conservative device researchers [4], [5].

In this paper, we want to examine three quantities that are often associated with nanowires, two of which are related to ballistic transport, and the third is how they will impact integrated circuits, where scaling is a major issue. In the next section, we discuss ballistic transport, first by discussing the very early work on space-charge-limited currents (in vacuum tubes), where the electrons which leave the cathode (source in our case) create a space-charge cloud, whose impact upon Poisson's equation is to create a barrier which then dominates the current–voltage characteristics. We will then turn to a brief discussion of whether or not ballistic transport is a useful concept for ultrashort gate length transistors in today's world. Then, we discuss the ballistic-to-diffusive crossover in two specific cases of nanowires—Si and InAs. That is, we will examine the crossover point between ballistic transport, where the resistance is dominated by Landauer's formula and the quantum resistance $h/2e^2$, and diffusive transport, where the resistance is given by Ohm's Law. Here, we examine just what length of wire is needed to ensure that the mobility is a viable concept (the diffusive limit), i.e., if the wire is too short, the transport is not collision dominated, and mobility has little meaning. Finally, we will turn to the question of scaling and examine whether nanowires will have an impact in future generations of integrated circuits.

II. Ballistic Transport

Ballistic transport in semiconductors is a relatively old idea. In this paper, by ballistic, we mean the lack of *any* scattering. It was discussed in regard to mesoscopic structures, where the mean-free path was comparable to the device size, in connection with the Landauer formula [6], but the ideas of ballistic transport are even older and are derived from the earliest treatments of transport in vacuum diodes. The Langmuir–Child law describes the ballistic transport of electrons in a thermionic diode, with space charge built up near the cathode (corresponding to our source in a MOSFET), after the two who developed it independently [7], [8]. Both of these men derived the expression for the current, finding that

$$I \sim \frac{V^{3/2}}{L^2} \tag{1}$$

and it is this relationship that has become known as the Langmuir–Child law. More recently, Shur and Eastman proposed that device performance could be improved by utilizing ballistic transport in ultrasmall channel length semiconductor devices [9] but also showed that the current in an n^+-n-n^+ device would have the same space charge and current relationship as that of (1). While the connection between the vacuum diode and the FET seems strange, the physics is quite similar. In the vacuum tube, the heated cathode emits a cloud of electrons, which accumulate just off the surface. When this excess charge is incorporated within Poisson's equation, a potential barrier to current flow is created, and the current is then largely controlled

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by the ability of the anode potential to vary this barrier (in a triode, the grid potential directly affects the barrier to control the current). In the semiconductor, electrons diffuse from the heavily doped source to the lightly n-type channel, creating this same excess charge. It is important to realize that any FET has a space-charge region, and potential maximum, between the source and the channel, and it is this that creates the connection to the Langmuir–Child law, as demonstrated by Shur and Eastman. There have been many suggestions that ballistic transport can occur in short-channel devices and might improve the performance [10], [11]. This remains a point of some dispute, but nearly all simulations show a number of equivalent effects. In a previous paper, we demonstrated that the onset of ballistic transport would lead to curves similar in shape to drain-induced barrier lowering—there would be an increase in the current and a loss of the obvious saturation [12]. In this section, we will outline the basic tenets that establish this point, that there is a move toward triodelike characteristic curves but that there still may be saturation at some point.

As mentioned already, true ballistic transport occurs in the complete absence of scattering. This is the case in vacuum tubes. There, electrons leave the cathode and form a space-charge layer adjacent to this region. The solution of Poisson's equation for the region between the cathode and the plate yields the Langmuir–Child Law (1). The importance of the Shur and Eastman result is that *exactly the same behavior* is found in n^+-n-n^+ semiconductor structures, which is the structure that is found in the n-channel MOSFET. As mentioned earlier, electrons move out of the source into the channel, creating a space-charge region at the source–channel interface. It is the modulation of this space-charge region by the gate potential that produces the normal device characteristics. One might expect then that the variation of the space-charge region by the gate (or by the grid in the vacuum tube) leads to a family of triodelike curves obeying (1) with different (gate voltage dependent) coefficients. Such triode curves would not be good for either logic or high frequency applications. In vacuum tubes, saturation behavior arises through the use of a screen grid, which isolates the actual plate (drain) potential from the space-charge region. In the quantum simulations of InAs nanowire MOS transistors with 30-nm gate length, this triodelike drain–current behavior has been observed to occur [13]. This behavior was also seen in [10], and we have also seen it in the semiclassical Monte Carlo simulations of InGaAs HEMTs with 10-nm gates [14]. Thus, it is clear that the tendency toward triodelike behavior as $I_D \sim V_{\rm DS}^{3/2}$ can be found as a signature of ballistic transport in FETs. Indeed, it was argued in [12] that drain-induced barrier lowering is one of the first indications of ballistic behavior and leads to qualitatively similar curves. However, one cannot argue just from the shape of the curves that ballistic transport is present but must carry out the comparison with, and without, scattering, as done in [10].

However, the argument goes as follows: Cannot we assure ourselves of saturation even with ballistic transport? Let us examine this question a little further. The current flow through the device is given by the normal expression

$$I = Wn_s e\nu = WC_{\rm ox}\nu(V_y)[V_G - V_T - Vy] \tag{2}$$

where W is the device width, $C_{\rm ox}$ is the gate capacitance, V_y is the channel voltage at position y, and $\nu(V)$ is the velocity achieved at this point. If we now average over the length of the channel, this becomes

$$I = \frac{WC_{\rm ox}}{L}\int_0^L \nu(V_y)[V_G - V_T - V_y]\,dy. \tag{3}$$

At this point, one normally inserts the mobility through $\nu = -\mu E = \mu(dV_y/dy)$, which converts the integral to one over the channel potential, and the normal FET curves are obtained. With ballistic transport, however, the velocity at a point is given by the energy (potential) which the carrier has gained or $\nu = [2eV_y/m]^{1/2}$, and the mobility has no meaning. However, at this point, the electric field is given in terms of the current and potential approximately as [8]

$$\frac{dV_y}{dy} = \alpha\sqrt{I}V_y^{1/4} \tag{4}$$

where $\alpha^2 = 8\pi[2e/m]^{1/2}$. Introducing this into (3) gives us

$$\begin{aligned} I^{3/2} &= \frac{WC_{\rm ox}\alpha}{8\pi L}\int_0^{V_D} V_y^{1/4}[V_G - V_T - V_y]\,dV_y \\ &= \frac{WC_{\rm ox}\alpha}{10\pi L}\left\{V_y^{5/4}(V_G - V_T) - \frac{5}{9}V_y^{9/4}\right\}. \end{aligned} \tag{5}$$

In fact, this does exhibit saturation behavior, at essentially the same drain voltage as for the nonballistic case, so that

$$I_{\rm sat} = K(V_G - V_T)^{3/2} \tag{6a}$$

with

$$K = \left[\frac{WC_{\rm ox}\alpha}{10\pi L}\frac{4}{9}\right]^{2/3}. \tag{6b}$$

Now, the saturation behavior is induced in exactly the same manner as in the normal FET—saturation occurs because the equilibrium charge density is pinched at some point in the channel, so that the current is set by the injection characteristics of the potential barrier at the source–channel interface. That is, *the occurrence of current saturation has little to do with the transport properties of the carriers in the channel itself*. Signatures of ballistic transport are then quite subtle, such as the change in the dependence of the saturation current on gate voltage in (6). However, based upon the observations found in the quantum and semiclassical simulations of ultrasmall FETs [10], [13], [14], this saturation may not be apparent in the characteristic curves, at least not to the extent seen in the long-channel devices.

The superlinear triodelike behavior discussed earlier describes at least the "linear" part of the curves below the saturation current. The actual details of the current behavior will vary with details of the theory. For example, the electric field in (4) arrives from one approach. Different approaches and assumptions will lead to a different formulation for the

field, but this will be a change in detail, not in the relevant physics of saturation in the channel. An interesting point is the $1/L^{3/2}$ behavior suggested by (5). Normal FETs normally show a $1/L$ behavior, and this difference might be important in establishing ballistic behavior but, as pointed out in many articles, the ballisticity of the transport is usually gate length dependent, so that this behavior is quite likely to be masked. Nevertheless, it is something that could be probed in simulation.

III. Ballistic-to-Diffusive Crossover

As pointed out earlier, there have been many assertions that ballistic transport is important in short-channel devices but becomes more important in nanowires and devices made from these nanowires. As remarked, this is seldom the real case [4], [5]. Recently, we actually developed a full quantum–mechanical simulator to study transport in nanowire FETs [15]. By inclusion of the self-energy corrections that arise from phonon scattering, we were able to investigate the transition from ballistic to diffusive transport [16], [17]. The approach taken utilizes an iterative solution approach to the wave function itself, with the iteration procedure based upon the Lippmann–Schwinger equation, which is an approach we have used to study quantum transport for years [18]. This approach is not a so-called "full band" approach, using parabolic bands, which is a point we return to in the next section. This transport solver is coupled to a self-consistent solver for Poisson's equation [16], and it is in this connection that the technique is more efficient than, e.g., nonequilibrium Green's functions. For the Poisson equation, one needs the local charge density at each grid point. With Green's functions, one has to perform an energy integration over the retarded Green's function at each grid point. With our approach, however, the density at each grid point is normalized to a value in the equilibrium contact, and this energy integration only needs to be done for the grid points in this contact region. The transport kernels themselves are comparable in terms of computational complexity, as both approaches require numerous matrix inversions that arise from Dyson's equation. Here, we will discuss results for silicon and indium arsenide nanowires.

To include electron-phonon scattering, as in most semiconductor theory, we treat the scattering as weak. Hence, we can use the Fermi golden rule expression, which is equivalent to a first-order non-self-consistent Born approximation. This permits us to derive scattering rates expressed in terms of the mode basis of the quantum wire waveguide. At that point, one does a transformation to the site basis, so that the effects of electron-phonon scattering now manifest themselves as local site corrections to the potential. Unlike the previous approaches whereby inelastic scattering was included by adding imaginary terms to the Hamiltonian, current is conserved using this approach. In the case of silicon, the scattering mechanisms included acoustic deformation potential scattering and intervalley scattering with both f- and g-type processes included. For the case of the InAs wire discussed below, the scattering mechanisms are acoustic phonons and polar optical scattering [19].

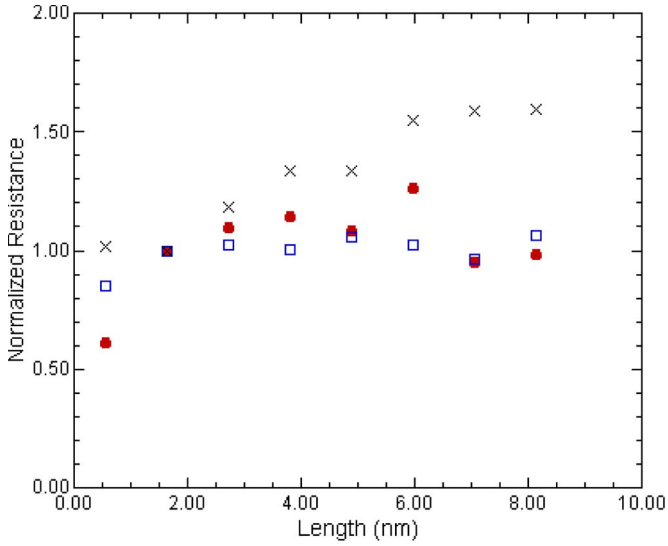

Fig. 1. Normalized resistance for three silicon nanowires as a function of wire length. The circles, squares, and crosses are for wires of widths 4.3, 6.5, and 9.7 nm, respectively.

We study the resistance versus length for a gated nanowire with a vanishing small drain voltage, so that the channel and density are essentially constant over the length of the transistor. In a ballistic device, the conductance is constant with length [6] and is given by the Landauer formula

$$G = \frac{2e^2}{h}N \tag{7}$$

where N is the number of transverse modes, e is the electronic charge, and h is Planck's constant. Here, there is no scattering; thus, the conductance is set by the number of 2-D modes propagating through the wire. Hence, the resistance will also be constant as the length is changed. On the other hand, for a diffusive device, the channel resistance should satisfy Ohm's law; hence, the resistance should increase linearly with wire length, which is a result that has been clearly demonstrated experimentally with InAs wires at 300 K [20].

A. Silicon Nanowires

The nanowire transistors studied in this paper had a silicon layer thickness of 6.51 nm, while the lateral dimension of the wires was varied. Oxide barriers were placed on either side of the channel to simulate the appearance of a hard wall boundary that would be present in an actual experimental system, as well as on top of the wire. The source and drain of the device are 36.93 nm wide and 27.15 nm in length. The source and drain of the device are discretely doped n-type with a doping concentration of 1×10^{20} cm^{-1}, while the channel is undoped. The quantum wire that forms the channel of the device has metal gates on three sides to form a trigate-type transistor. The gate oxide thickness (SiO_2) of this device was 1 nm.

In Fig. 1, we plot the normalized resistance of three wires at 100 K. These wires were normalized to the resistance value at a length near 2 nm in order to plot them together (the values of the resistances are 3.7, 3.3, and 1.4 kΩ for the 4.3-, 6.5-, and 9.7-nm wires, respectively). It is clear that the resistance is

mainly independent of length except for the smallest wire. Even in this case, the increase is not proportional to the wire length, and the increase is most likely due to some localization occurring in the wire. There is a drop-off in most cases for lengths below 2 nm. To understand what is special about 2 nm, we previously performed a calculation for the ideal ballistic case with a *perfect* wire (without any scattering at all from phonons or impurities) but with simple thermal broadening included using Fermi functions with $T = 300$ K [17]. A length of 2 nm is the approximate length for which the resistance saturates in the ballistic case. Beyond this length, the wire acts as an ideal quantum point contact due to the narrow wire inserted between two wide source and drain contacts. In this case, the transmission is quantized and proportional to the number of propagating modes in the wire. The effects of this quantization are evident even with the thermal broadening. However, at shorter lengths, evanescent wire modes that have not decayed can tunnel from the source to the drain, destroying the conductance quantization and decreasing the resistance. Thus, only wires longer than 2 nm (in silicon) show clear wire-like behavior. Thus, at low temperatures, where the phonons are not well excited, the wires show clear ballistic behavior.

In contrast to the aforementioned behavior, we show the resistance as a function of wire length for two wires at 300 K (Fig. 2). At this temperature, the phonons are fully excited and dominate the transport. While there is some variation in the data points, it is clear that the increase in resistance is essentially proportional to the length of the wire. This is clear evidence that this transport is not ballistic but is fully diffusive in expectations of Ohm's law. Thus, at room temperature, we find that the resistance deviates from the ballistic prediction, even down to the length at which the wire becomes a true waveguide. This is in keeping with the predictions earlier of Kotlyar *et al.* [5], which were mainly based on a semiclassical approach. Thus, it seems clear that ballistic transport is unlikely to be seen in silicon transistors at room temperature down to extremely short gate lengths, probably below 2–3 nm.

One might ask how this fits into the expectations based upon the mobility of Si. If we take a mobility value of 500 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ for the electrons in [100] channels, then the *average time* between collisions is 54 fs. At the thermal velocity, this leads to an expectation of an *average* mean-free path of some 7 nm. However, this neglects the role of small angle scattering, and the actual scattering rate, which is larger than the average. Even with intervalley phonon scattering, we expect the induced mixing between multiple subbands to produce a coherence breaking effect that leads to much shorter ballistic lengths. Thus, it is fully expected that the ballistic behavior would be limited to wire lengths of only 2–3 nm.

Finally, we should remark that these results were obtained using the analytic parabolic bands from bulk silicon. At some point, these become quite modified by the confinement and small size of the wire, and a better approach is needed. The point at which this occurs is somewhere in the 3–5-nm range (opinions vary as to the limit). Thus, we expect the results of the two larger wires to not be susceptible to this need, but the smallest wire is clearly pushing the limit of the analytical band model.

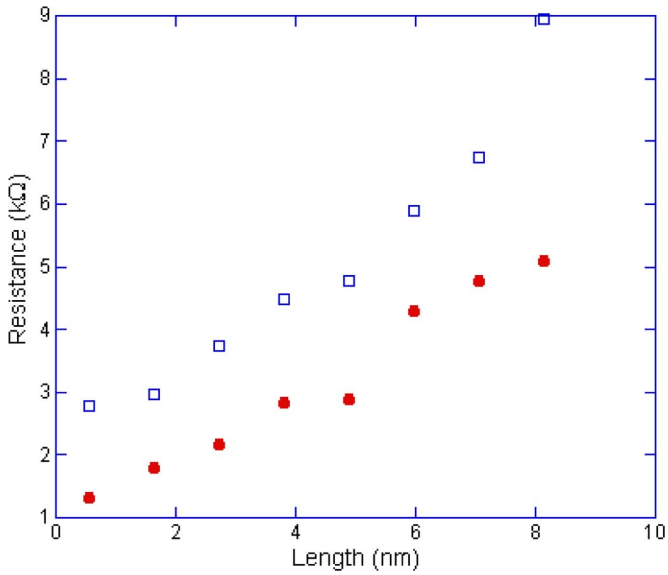

Fig. 2. Resistance as a function of length for two wires at 300 K. The squares and circles are for wires of 6.5 nm and 9.7 nm, respectively. The resistance has not been corrected for the contact resistance of the source and drain.

B. InAs Nanowires

A similar approach was taken to simulation of an InAs nanowire. In this case, there exist experimental data for measurements of this ballistic-to-diffusive crossover. Zhou *et al.* [20] grew these wires by metal–organic CVD using Au colloidal particles to seed the wire growth on SiO_2. The wires were unintentionally doped n-type. The wires were subsequently placed on an oxidized Si substrate and contacts applied. A conducting AFM was used to measure the resistance between one contact and a point along the wire, so that resistance versus effective transport length could be measured. They found that drift-dominated transport at 300 K began for lengths on the order of 200 nm. This is much longer than for silicon but the effective mass is much less than that in Si, and the scattering by polar modes is also less effective than the intervalley rates in Si. Thus, it is not surprising that such a long ballistic length can appear in this high mobility material.

We used our quantum transport simulator discussed earlier to simulate such InAs nanowires. Our wires had a cross-sectional area of 30×30 nm and were doped to 7×10^{16} cm^{-3}. The contact regions were doped slightly higher at 1×10^{17} cm^{-3} and were slightly wider (35 nm) than the wires. Scattering by ionized impurities, acoustic and polar mode phonons, and by intervalley phonons to higher lying valleys of the conduction band was included. A source–drain bias of 1 nV was assumed. A full self-consistent calculation was performed, and the resistance versus wire length was determined. The general resistance of the wire in the ballistic regime was about 4.2 kΩ, which is considerably less than the experimental wires studied [20] but is within the range of reported resistances by these authors (their measurements were complicated by contact resistances as well). The calculated variation of the wire resistance with wire length is shown in Fig. 3. Here, the transition to diffusive behavior occurs around 180 nm, slightly less than the experiments, but within the error of both the experiment and the theory. At

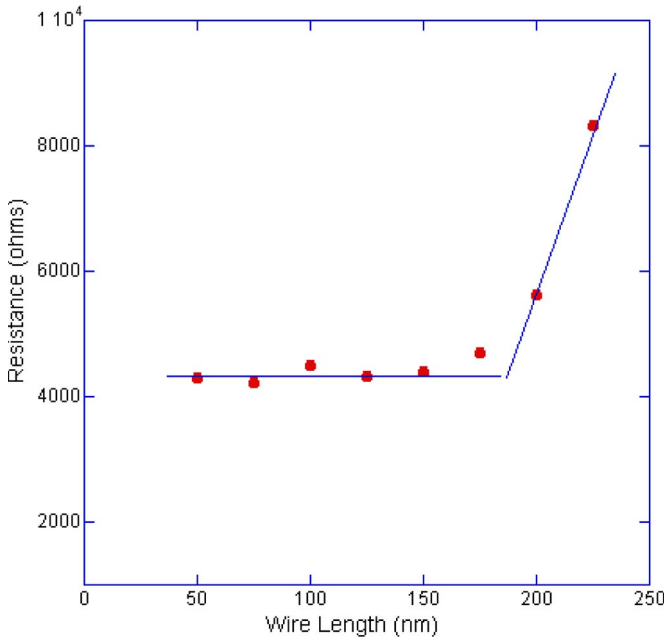

Fig. 3. Variation of wire resistance versus wire length for an InAs nanowire (details are discussed in the text).

longer lengths, the resistance appears to rise more rapidly than linear in wire length, but there is insufficient data to make this distinction (and we should remark that computations at these lengths take a considerable time).

It is apparent from these results, as well as those of the Si nanowires reported earlier, that measurements of quantum transport, including detailed self-energies for the scattering processes, can be used to estimate the real transport in such structures. Moreover, where experimental results are available, the simulations provide a reasonably good agreement with these experiments.

IV. Impact of Nanowires on Circuits

Moore's law has traditionally explained the growth in chip density, which is achieved through three factors. The first of these, and the most obvious, is the reduction in feature size, with the minimum feature—the gate length—being essentially one-half of the node dimension. The new 45-nm node chips have gate lengths in the 20–22-nm range. The second factor traditionally has been a continued increase in the size of the die (the chip), and this has led to an increase in the size of the wafer itself, which today is 300 mm in diameter. However, for the past few years, this has not been occurring, as faster operation has been obtainable through using multichip modules for the microprocessor. The new 45-nm node chips have a die size of only 107 mm^2 for the dual core version, according to information available on the Intel website. Moreover, chips have remained roughly at this size for almost a decade. The third factor, and one to which we will return later in this paper, is the role of circuit cleverness, whereby novel designs for the functions integrated on the chip can lead to reductions in the required area.

With the ending of the increase in die size, it is apparent that the continued growth of integration density must rely even

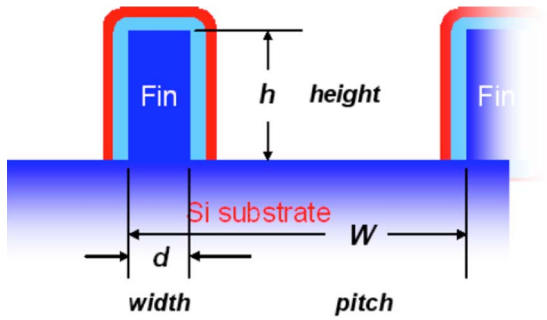

Fig. 4. Descriptive picture of placing FinFETs on Si surface.

more on the reduction of feature size. For the maintenance of the same growth rate, we now need an even greater reduction in the critical dimensions. However, it has been recognized for years that the real driving force for Moore's Law and increased density is basically economic, as it is the continued reduction in cost per function built into the integrated circuit that drives the technology. With the increased pressure on dimensional reductions, it becomes quite clear that *any new technology must not incur an increase in chip area*. This puts an important economic limitation on the possible implementation of new device concepts.

Each new device concept, whether FinFET or nanowire, has been championed as the replacement for CMOS logic circuits. In fact, many such saviors have come and gone, yet the reliable CMOS continues to be scaled and to reach even higher performance levels. It is important, then, to try to ascertain what questions must be asked if a new technology is to become useful. The answer to this question arises on several levels. First, and perhaps most foremost, is that any new technology must ride upon the wave of the exceedingly large investment that has been made in CMOS integrated circuits. Furthermore, the most likely scenario for a new transistor technology is one which will supplement the current CMOS circuits to provide enhanced performance for some part of the overall architecture of the computational chip. If a new technology is to supplement the current approaches, then it must satisfy Moore's law, as well as the economics—e.g., the use of Si real estate must be optimized if the cost per function is going to continue to be reduced.

The economical use of Si area can be illustrated by considering dimensions for the FinFET. In Fig. 4, we plot a single FinFET, in an array of FinFETs, and describe the various dimensions of this structure. Clearly, the peripheral distance, e.g., the net gate width of the transistor, is simply $2h + d$. Now, if we are to use the Si area to maximal effect, then we must have

$$2h + d > W \tag{8}$$

where W is the *pitch* of the transistors. Only if this equation is satisfied do we gain in Si area by use of the FinFET. However, for the case of the FinFET, this becomes a relatively easy condition to satisfy.

However, this same logic must be applied to concepts in which nanowires are used on the Si surface. This will be the case, whether the nanowires are self-assembled in vertical growth, and subsequently placed on the surface, or are patterned

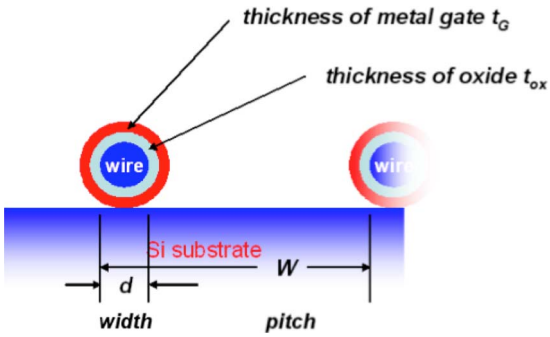

Fig. 5. Descriptive picture of a nanowire on a Si surface.

directly in the Si surface. It will also be the case whether the nanowires are CNTs, Si nanowires, or any other semiconductor nanowire. We illustrate the geometry in Fig. 5. The wire itself can be assumed to have a diameter d, but to this, the thickness of the oxide layer $t_{\rm ox}$ and the thickness of the gate layer t_G must be added. Thus, to fit the wires within the pitch W, we must have

$$d + 2(t_{\rm ox} + t_G) < W. \tag{9}$$

This requirement is just to fit the wires onto the planar surface. However, we cannot waste surface area—we must satisfy the law regarding the cost of Si real estate. Hence, we must have more transistor periphery than W or

$$\pi d > W. \tag{10}$$

These two equations then set a limit on how small the nanowire can be, which is given by

$$d > \frac{2(t_{\rm ox} + t_G)}{\pi - 1}. \tag{11}$$

Generally, the gate thickness must be about 3 nm or larger. If the oxide is then 2 nm thick, we are faced with the fact that the wire must have a diameter of 5 nm or more. However, this assumes a gate-all-around geometry. If the gate only covers half of the wire, then the minimum diameter grows to 10 nm. Thus, we cannot make use of extremely small diameter nanowires. Note that this is a requirement just from Moore's law on the cost of Si real estate. It does not take into account any performance improvement in the nanowire. Indeed, for the performance to affect this argument, the nanowire would have to offer orders of magnitude performance enhancement over Si.

The conclusion from this is that horizontal nanowires will probably not compete well with FinFETs. Certainly, there is an argument that the nanowire can offer volume inversion, which will pull the carriers away from the oxide interface (and raise mobility), but this can also occur in well-designed FinFETs [21]. Does this mean that nanowires have no future? No, instead, it means that the proper technology to incorporate these structures into high performance devices has not been utilized in most cases. There is a third important factor in increasing chip device density, and that is clever circuit design; it is here that the real strength of the nanowires may appear. A modern integrated circuit chip is a dense array of many different materials. While most of the devices sit at the Si surface, in the bottom-most level, there are several levels of metals and insulators lying above this. In fact, one of the most important uses of nanowire transistors may well be as vertical switches between levels of metal in these upper layers. The development of a vertical nanowire transistor, which can be integrated within the metallization layers of the integrated circuit, will allow for active system reorganization, and this can open the way to many novel new applications [22].

There have been developments in the use of vertical nanowires, not the least of which is as field emitters. However, the idea of vertical nanowire interconnects, or of transistors, was discussed already some time ago by Graham *et al.* [23]. However, a great many vertical nanowire transistors have already been demonstrated, and these can be situated by use of the seed crystal in VLS growth. However, challenges remain in creating arrays of such wires with growth at well-determined points and, more importantly, in the required new design paradigms that will be needed for the circuit layout. Questions as to which part of the circuit should be vertical transistors and how to implement a reconfigurable architecture are still formidable challenges that must be addressed in the future.

V. Conclusion

While nanowires provide considerable novelty, and are quite useful for studies of the physics of transport in constrained systems, their applicability to future integrated circuits remains under investigation. On the other hand, they provide some new and novel applications (such as 3-D transistors), which are unique to these nanowires. Beyond the integration, however, there are considerable opportunities in, e.g., sensor applications, which we have not discussed in this paper. Instead, in this paper, we have focused upon just three issues: ballistic transport in FETs, the ballistic-to-diffusive crossover in nanowires, and the impact which nanowires may have in integrated circuits.

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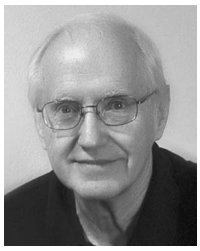

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