Vorticity and Quantum Interference in Ultra-Small SOI MOSFETs

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***Abstract*—As scaling and performance needs of industry has continued, silicon-on-insulator technology appears to be a viable option. However, the small sizes of these structures require a quantum treatment for the transport. In this paper, we present results from a full three-dimensional (3-D) quantum simulation and describe the effects of quantum interference and vorticity arising from the discrete nature of the dopant atoms. In wide (∼18 nm) channel devices, as the electrons travel from the source to the drain of the device, vortices in their motion form, based on the 3-D positions of the dopant atoms in the device. For a narrow-channel device (∼8 nm), the quantum interference effects are exacerbated, as seen in the output currents. The vorticity of the electron density is not suppressed at low drain biases. However, at higher drain biases, the vortices are washed out due to increased interaction with the channel dopants and increased carrier energy.**

***Index Terms*—MOSFET, quantum interference, silicon-on-insulator (SOI), vorticity.**

I. Introduction

IT IS a well know fact that the semiconductor industry is aggressively scaling its MOSFET technology to meet future demands. Looking beyond 2010, there is some question as to what will be the next transistor technology. While progress on the MOSFET has been quite steady, silicon-on-insulator (SOI) technology has been shown to offer better performance over traditional silicon technology with better scaling. Recent developments have demonstrated that it is possible to fabricated MOS devices in an SOI environment with channel widths as small as 2 nm [1]. These devices are coupled in all three directions and must be treated as such without resorting to the separation of one or more dimensions in terms of basis expansions. In this paper, we utilize a fully quantum mechanical three-dimensional (3-D) self-consistent device simulation tool based on the scattering matrix technique [2]. Here, we examine the effects of transport and charge discreteness in wide (∼18 nm) channel devices and narrow (∼8 nm) devices.

II. Descirption of the Device

We consider two typical devices shown in Fig. 1. Both are SOI MOSFETs that have a unique construction. In general, we have a wide source and drain region, which are doped 6×10^{19} cm^{-3} N-type. The dimensions of the source and the drain are 18.47-nm wide, 10.32-nm long, and 6.51-nm high (integer multiples of the Si atom spacing) corresponding to the thickness of the silicon layer. The channel of our device is a P-type region, which has been doped 5×10^{18} cm^{-3}. In the first device, Fig. 1(a), the channel region is 8-nm wide, 9.77-nm long, and 6.51-nm high. The source and drain of this device have an exaggerated size to exacerbate the interaction of the modes excited in the source with the constriction present at the source–channel interface. It should be noted that on either side of the narrow channel, we have included oxide regions to confine the density rather than impose hard wall boundary conditions. The second device, as shown in Fig. 1(b), has identical source and drain dimensions, as well as doping concentrations for the different regions as the narrow MOSFET device. The difference between the two devices comes from the fact that we remove the oxide constrictions from the sides of the channel to form a channel with a width of 18.47 nm corresponding to the sizes of the source and drain regions.

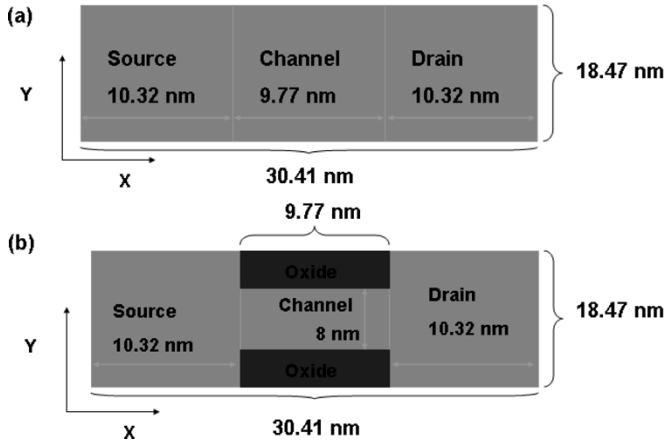

Fig. 1. (a) Device schematic for the wide-channel device. (b) Device schematic for the narrow-channel device.

The exact device dimensions are included in the simulations due to the dopant inclusion routine. Once the dopants are distributed, they are mapped back to the computational lattice and the resultant potential profile [3] is shown in Fig. 2.

Adding this potential to the Hamiltonian has the effect of adding the bare coulomb interaction with the dopants in the device. It is not appropriate to include a model such as Brooks–Herring or Conwell–Weisskopf, as the screening of the electrons is accomplished by performing the simulation on a real space grid. Further, these simulations are performed on a quantum basis and the screening approximations are classical. In addition, all simulations are performed at 300 K and ballistic transport is assumed. A nonuniform adaptable mesh has been

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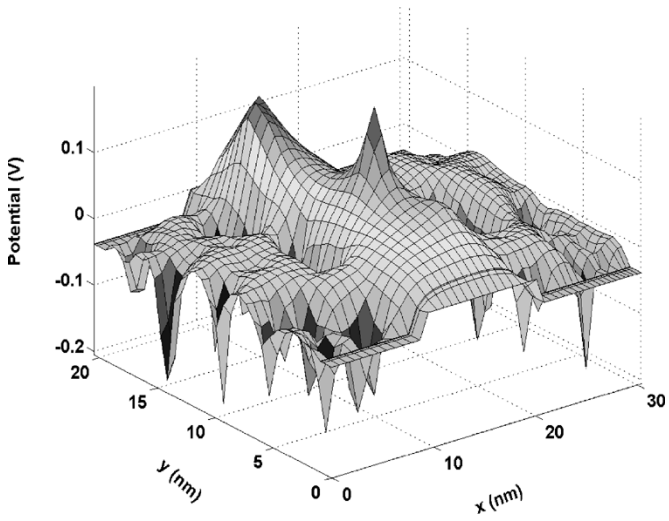

Fig. 2. Potential profile for the wide-channel SOI MOSFET taken at a depth of 7 nm from the surface of the device.

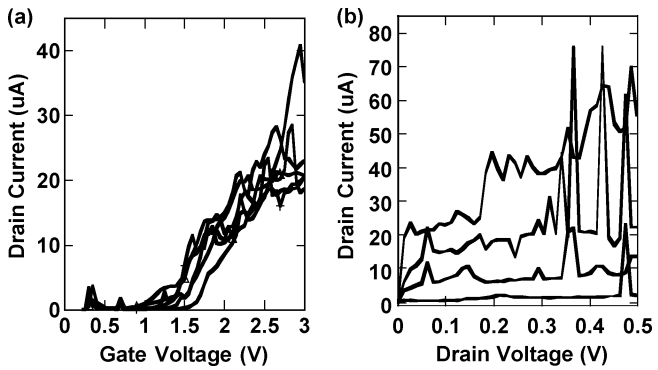

Fig. 3. (a) $I_d - V_g$ curves for six different dopant distributions for the wide-channel case for $V_d = 10$ mV. Here, we see the results of the quantum interference. The electron density interacting with the acceptors causes the observed spikes. (b) $I_d - V_d$ curves corresponding to the wide-channel SOI MOSFET devices. From bottom to top, the gate voltages are 1.5, 2, 2.5, and 3 V. The peaks are evidence of the formation of resonant levels in the channel.

implemented to ensure that all of the applied biases are kept within the artificial band structure created by the discretization of the Schrödinger equation. This ensures the physics is correct, while conserving grid points and computation time. The adaptable mesh is not utilized when sweeps of the gate voltage are considered, as the mesh required is close to uniform in all three dimensions. However, when the drain voltage is swept, the mesh is highly nonuniform in all three dimensions.

III. Results for the Wide-Channel SOI MOSFET

A. $I_d - V_g$ Characteristics

We now examine results obtained from the simulation of the wide-channel SOI MOSFET (device 2). The $I_d - V_g$ curves obtained from six different dopant distributions are shown in Fig. 3(a). The spikes present in the plots give an excellent example of the quantum interference effects that occur in this system. When the discreteness of the doping is taken into account, the landscape of the potential is drastically altered [3]–[5]. The potential peaks now present in the channel set up additional reflections in the device, as well as forming resonant

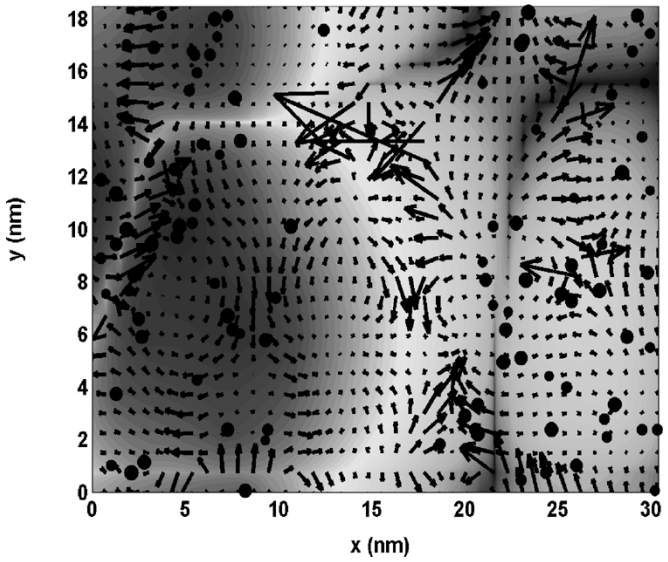

Fig. 4. Electron density corresponding $V_g = 0.5$ V. The arrows represent the corresponding velocity field, while the dots represent the locations of the dopants. Larger dots correspond to atoms closer to the surface, while smaller dots are deeper in the device.

levels. These effects lead to the observance of the spikes in the curves shown in Fig. 3(a). Moreover, the position of the dopants in the channel also has a profound effect on the shape of the curves as, when the acceptor atoms are placed more toward the source side of the channel, the interaction is much stronger and produces more peaks in the curve. Further, we also see device-to-device variation in the threshold voltage due to the differing dopant distributions, as seen in a previous study [3]. In Fig. 3(b), we plot the $I_d - V_g$ curves associated with one of the wide-channel devices. Additional peaks in the current give further evidence of the formation of resonant levels in the channel based on the position of the dopants in the channel. We conclude that this resonant behavior persists even at greatly elevated drain voltages.

In Fig. 4, we examine the electron density corresponding to a gate voltage of 0.5 V and a source–drain bias of 10 mV. It should be noted that, in the plots of electron density, we only consider the source driven density. However, the velocity field patterns were computed using both positive and negative k-states. To calculate the velocity field pattern, we begin by writing the wave function in the following form:

$$\psi = \mathrm{Re}^{i\frac{S}{\hbar}}. \tag{1}$$

We may then calculate the velocity flow pattern [6] as

$$v(\vec{r},t) = \frac{\nabla S(\vec{r},t)}{\hbar} = \frac{\hbar}{m^*}\frac{\mathrm{Im}(\psi^*\nabla\psi)}{|\psi|^2}. \tag{2}$$

Once complete, we see a turbulent density flow pattern in the wide-channel device. The density is plotted over the location of the dopant atoms and the corresponding velocity field pattern in then superimposed. First, the density preferentially sits on the locations of donors in the source and drain of the device. This is a direct result of the self-consistent calculations as, without the self-consistency, the density would simply consist of several blobs, which do not see the energetically preferential sites.

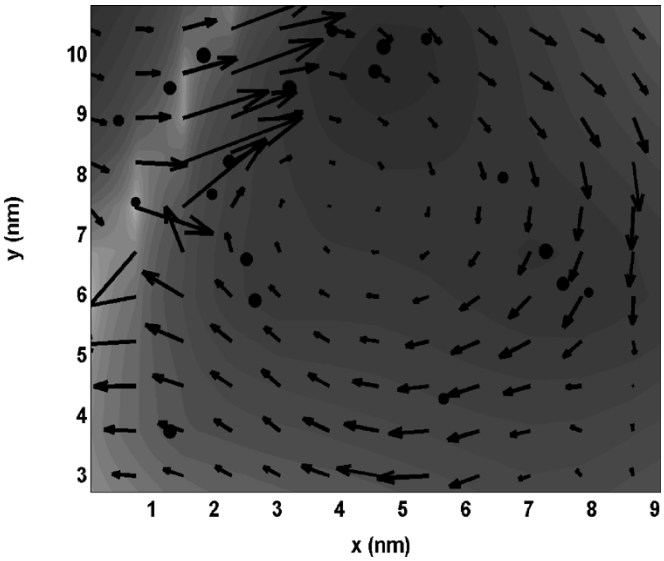

Fig. 5. Close-up view of the vortex formed in the source of the wide-channel SOI MOSFET at $V_g = 0.5$ V.

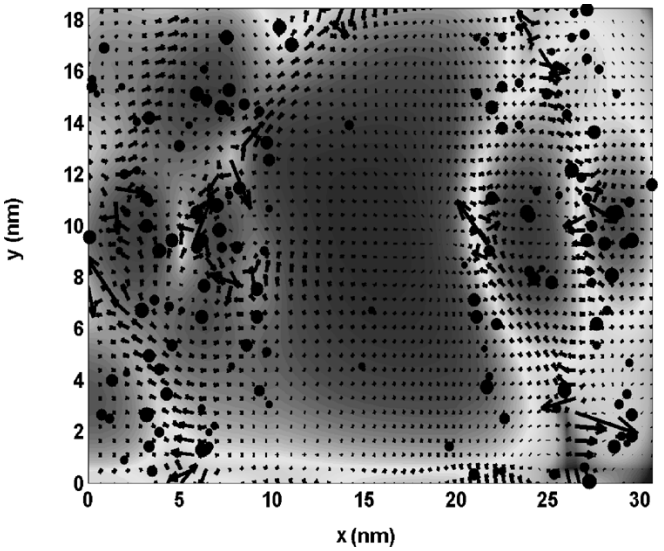

Fig. 6. Electron density corresponding $V_g = 2.25$ V and $V_d = 75$ mV. At higher drain voltages, the vorticity persists if the proper distribution of the dopant atoms is correct.

In certain situations, the donors may form a circular pattern at approximately the same depth in the device. When this occurs, a ring of lower potential forms and the flow forms a vortex in the middle of these circularly distributed donors, as seen in Fig. 5. This is the first observance of dopant induced vorticity. Further, we can also see the density being repelled from the centrally located acceptor in the channel of the device.

While it is clear that vortices may form depending on whether the dopant distribution criteria are satisfied, it is natural to wonder if this behavior persists at higher drain voltages. To study this, the electron density is once again plotted in Fig. 6, but for a source–drain bias of 75 mV. Here, we see that, even at higher drain voltages, when the dopant configuration is correct, a vortex will form in the depressed region of potential created by the dopants. In the simulations of the wide-channel device, we find the formation of the vortices in the source and

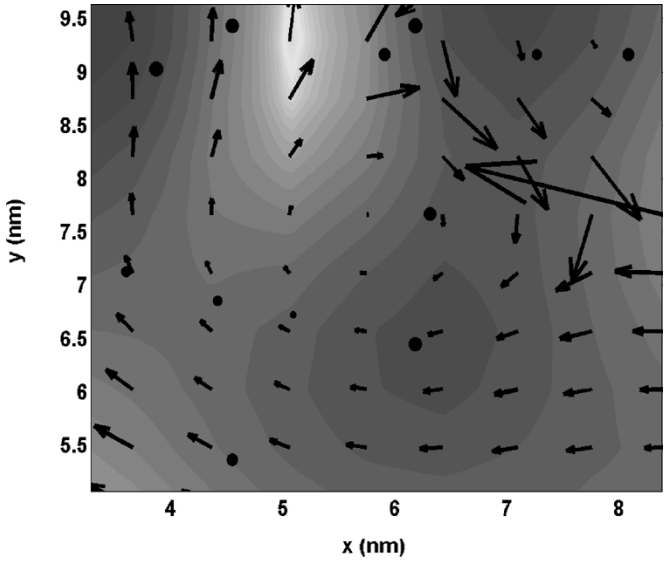

Fig. 7. Close-up of the vortex formed in the source of a wide-channel device with $V_g = 2.25$ V and $V_d = 75$ mV.

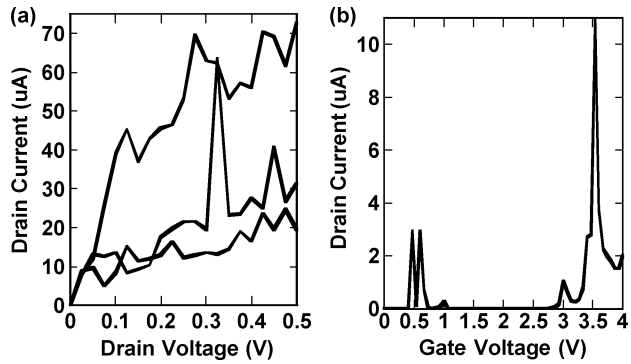

Fig. 8. (a) $I_d - V_d$ curves corresponding to three different gate biases for the narrow-channel SOI MOSFET devices. From top to bottom, the gate bias is 2.5, 3, and 3.5 V. (b) Typical $I_d - V_g$ curve for the narrow-channel device.

drain, but due to the dependence on the location of the dopants, we did not find any vortices in the channels of the devices. A view of the vortex in the source region is shown in Fig. 7.

IV. Narrow-Channel Device Results

Fig. 8(a) and (b) shows the current–voltage relations for the narrow-channel device. Here, we see the expected increase in the threshold voltage due to the decrease in the channel size. We also observe a reduced current flow through the constricted channel. Additionally, we observe sharper resonances, due to the interaction with the discrete dopants, than in the wider device. This is due to the more clearly defined levels in the channel for the density to tunnel through in the channel.

When we examine the electron density and velocity fields for the narrow-channel device using only the forward propagating density, we find the formation of vortices at low applied biases. In Fig. 9, we plot the forward propagating density in the narrow device for a gate voltage of 0.93 V. Here, we find that vortices form in both the source and drain of the device. While the interference has been increased due to the different channel access geometry, this does not wash out the vortex formation shown

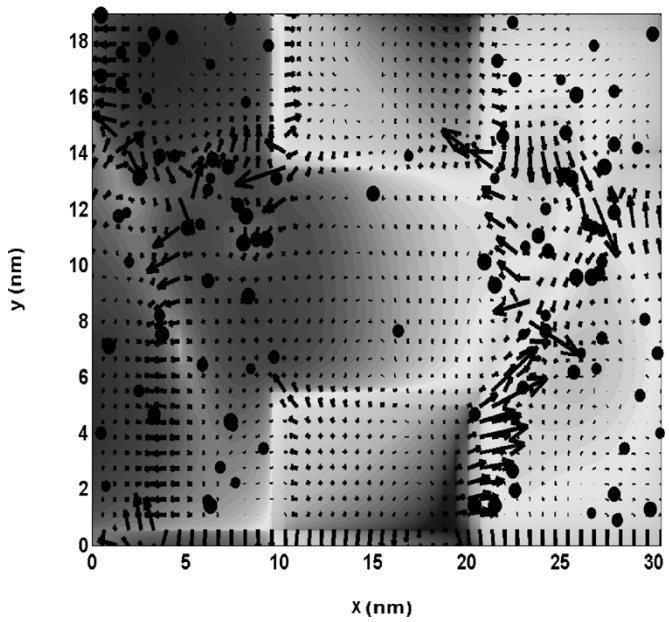

Fig. 9. Electron density corresponding to $V_g = 0.933$ V and $V_d = 0.010$ V. Vortices form in the source and drain of the device corresponding to the preferential sites set up by the distribution of dopant atoms.

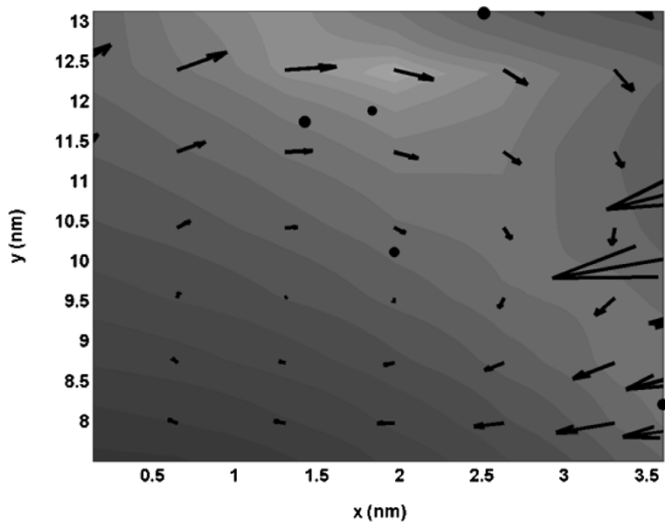

Fig. 10. Close-up of vortex formed in the source of the narrow SOI MOSFET at a gate voltage of $V_g = 0.93$ V.

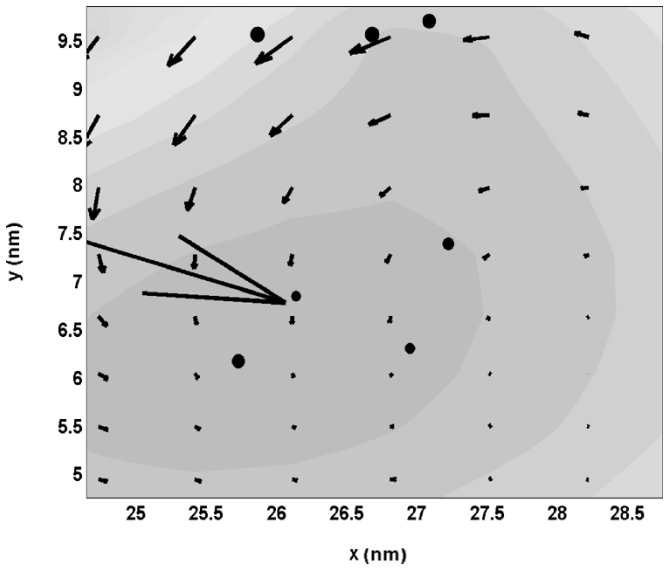

Fig. 11. Close-up of vortex formed in the drain of the narrow SOI MOSFET at a gate voltage of $V_g = 0.93$ V and drain voltage of $V_d = 0.01$ V.

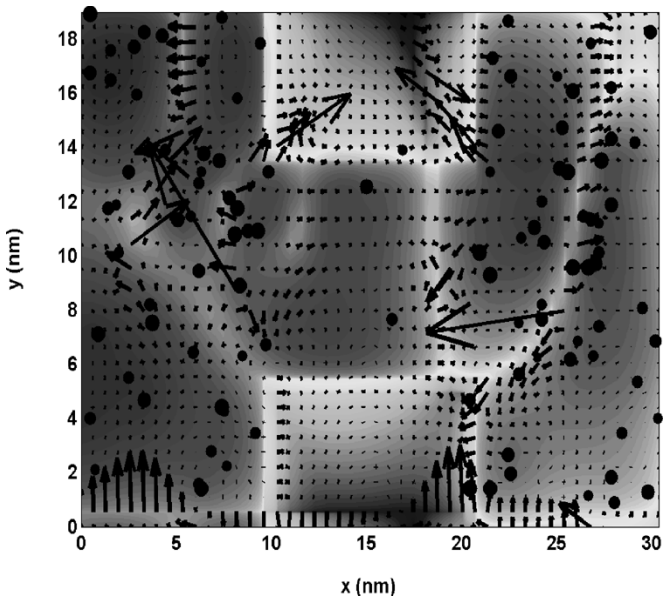

Fig. 12. Electron density corresponding to $V_g = 2.93$ V and $V_d = 0.475$ V. At higher gate biases, the increased interaction with the channel dopants washes out the vortices in the source and drain of the narrow SOI MOSFET.

in Figs. 10 and 11. This is not too difficult to understand as the carriers are only slightly pushed from equilibrium. Therefore, the interaction that the carriers have with the dopants is maximized. We now proceed to determine the existence of vortices at higher drain biases. As the drain voltage is increased on the device, the electrons begin to enter the channel and are accelerated by the channel field. This fact leads to several modifications in the electron density not seen in the low bias cases. We get stronger interactions with the channel dopants. This causes additional disruptions in the electron flow leading to some additional reflected density. We also have more energetic electrons in the drain of the device, which are not easily trapped in the potentials caused by the donors. The result is that the vortices are washed out in narrow-channel devices at high applied biases. This is shown in Fig. 12, where we plot the electron density for the forward propagating density at a gate bias of 2.93 V with a drain bias of 0.475 V.

V. Conclusion

These results outline the impact of quantum interference and the existence of discrete dopant induced vortices in SOI quantum-wire MOSFETs. The formation of these vortices arises from formation of a ring of preferential sites in the source and drain in which the density circulates. In wider devices, the vortices appear at a variety of gate and drain biases based on the position of the dopants and the corresponding interactions therein. In the latter, we find that, at low drain biases, vortices form in the source and drain. However, as the drain voltage is increased, additional reflections from the channel dopants and

additional electron energy disrupt the velocity flow patterns in the source and drain washing out the vortices. It should be noted that these are not the only mechanisms for washing out the vortices. If dissipation were to be included in these simulations, the vortices should be washed out. This removal of the vortices would be primarily due to the fact that the energies of the carriers are modified and, therefore, will not become trapped by the potential landscape.

In summary, we have used a full 3-D quantum mechanical simulation approach to study the dynamics of current flow in quantum-wire SOI MOSFETs. The ballistic nature of the transport results in interesting nonlinear flow that has not been previously reported in such devices.

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