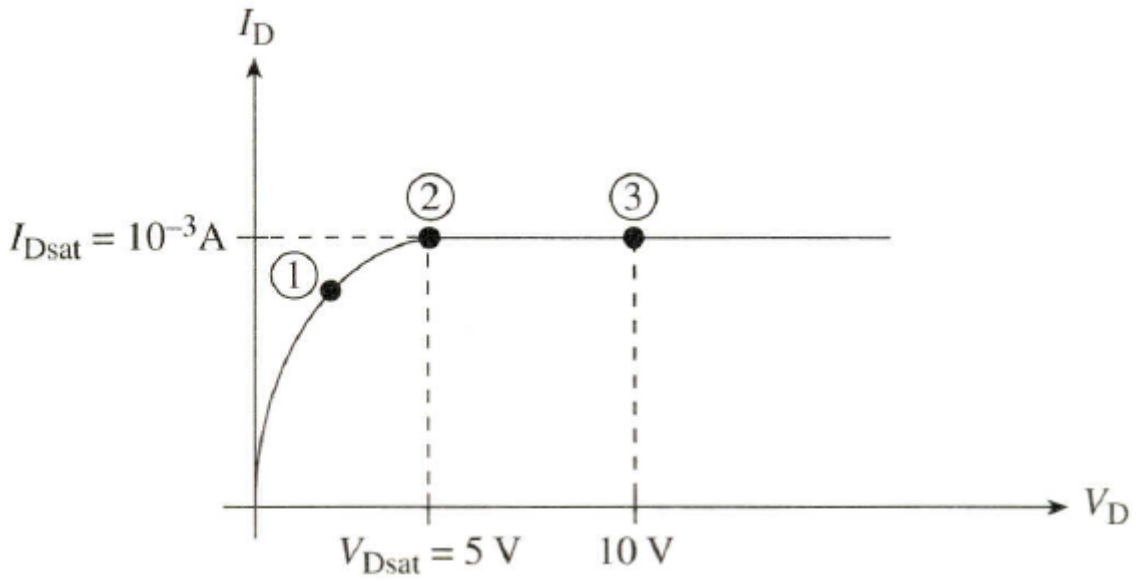
Problem # 1:

Plot and label the C-V curve of a PMOS capacitor with P^+ gate, substrate doping of $N_A = 6x10^{16}$ cm^{-3} and $SiO_2 = 3$ nm.

Problem # 2:



An I_D - V_D characteristic derived from an ideal MOSFET is shown above. Note that $I_{Dsat} = 10^{-3}$ A and $V_{Dsat} = 5$ V for the given characteristic.

a. Sketch the inversion layer and depletion region inside the MOSFET corresponding to point 1 on the graph. Show and label all parts of the transistor.

b. Given a turn-on voltage of $V_T = 1$ V, what is the gate voltage one must apply to the MOSFET gate to obtain the pictured characteristic?

c. if $x_0 = 0.1$ μm, what is the inversion layer charge / cm^2 at the drain end of the channel when the MOSFET is biased at point 2?

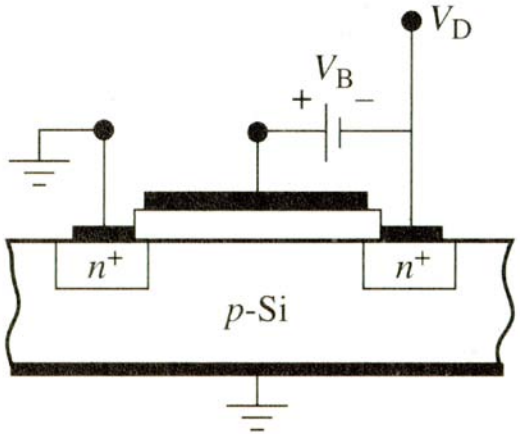
d. Suppose the gate voltage is readjusted so that $V_G - V_T = 3$ V. For the new condition, determine I_D if $V_D = 4$ V.

e. If $V_D = 0$ (i.e. the drain is shorted to the source and back), sketch the general shape of C_G (gate capacitance) versus V_G to be expected from the MOSFET.

Problem # 4:

The most widely encountered MOSFET characteristics are a plot of I_D versus V_D with V_G or V_G-V_T held constant at select values. An alternative plot of I_D versus V_G or V_G-V_T with V_D held constant at select values is sometimes useful. Sketch the shape of the I_D versus V_G-V_T characteristics to be expectede from an ideal n-channel MOSFET. Specifically show the characteristics corresponding to V_D = 1, 2, 3, and 4 V. Explain how you arrived at the sketch.

Problem # 5:



Suppose a battery $V_B > 0$ is connected between the gate and drain of an ideal n-channel MOSFET as pictured. Sketch the I_D versus V_D ($V_D > 0$) if $V_B = V_T/2$ and $2\ V_T$.