Problem # 1:

Plot and label the C-V curve of a PMOS capacitor with P⁺ gate, substrate doping of $N_D = 5 \times 10^{17}$ cm⁻³ and SiO₂ = 2 nm.

$$C_{ox} = \frac{\varepsilon_{ox}}{d} = \frac{3.9 \times 8.85 \times 10^{-14}}{2 \times 10^{-7}} \text{ F/cm} = 1.726 \times 10^{-6} \text{ F/cm}$$

$$\phi_F = \frac{k_B T}{q} \ln \left( \frac{N_D}{n_i} \right) \approx 0.45 \text{ V}$$

$$V_{FB} = \frac{1}{q} \left( \frac{q \gamma_{Si} + E_g}{\varepsilon_{Si}} - \frac{1}{q} \left( \frac{q \gamma_{Si} + E_g/2 - \phi_F}{\varepsilon_{Si}} \right) \phi_{gate} \right)$$

$$V_{FB} = \frac{1}{q} \left( \frac{E_g/2 + \phi_F}{\varepsilon_{Si}} \right) \approx 0.55 \text{ V} + 0.45 \text{ V} = 1 \text{ V}$$

$$V_T = V_{FB} - 2 \phi_F - \frac{1}{C_{ox}} \sqrt{2 \frac{q^2 N_D \varepsilon_{Si} 12 \phi_F}{\varepsilon_{Si}} = 1 \text{ V} - 0.9 \text{ V} = \sqrt{\frac{2 \times 1.6 \times 10^{-19} \times \gamma \times 5 \times 10^{17}}{1.726 \times 10^{-6}} \frac{17}{3} \frac{\gamma_{Si}^2}{\varepsilon_{Si}}}$$

$$V_T = 1 \text{ V} - 0.9 \text{ V} - 0.226 \text{ V} = -0.126 \text{ V}$$

$$C_{max} = C_{ox} = 1.726 \times 10^{-6} \text{ F/cm}$$

$$C_{min} = \left( \frac{1}{C_{ox}} + \frac{W_{max}}{\varepsilon_{Si}} \right)^{-1}$$

$$C_{min} = \left( \frac{1}{C_{ox}} + \sqrt{\frac{2 \gamma_{Si}^2}{q^2 N_D \varepsilon_{Si}}} \right)^{-1} = 1.923 \times 10^{-7} \text{ F/cm}$$
Problem #2:

An $I_D - V_D$ characteristic derived from an ideal MOSFET is shown above. Note that $I_{D_{sat}} = 10^{-3}$ A and $V_{D_{sat}} = 5$ V for the given characteristic.

a. Sketch the inversion layer and depletion region inside the MOSFET corresponding to point 1 on the graph. Show and label all parts of the transistor.

Since $V_D > 0 \rightarrow$ N-channel. At point #1, the MOSFET is biased below saturation and the channel is not punched off.

b. Given a turn-on voltage of $V_T = 1$ V, what is the gate voltage one must apply to the MOSFET gate to obtain the pictured characteristic?

\[
V_g = V_{D_{sat}} + V_T = 6 \text{ V}
\]

We use square law theory: $V_{D_{sat}} = V_g - V_T$

\[
Q_N (L) = 0 \text{ } \epsilon / \text{cm}^2
\]

c. If $x_0 = 0.1 \mu$m, what is the inversion layer charge / cm$^2$ at the drain end of the channel when the MOSFET is biased at point 2? Point #2 corresponds to punch-off point. If this is true then

\[
Q_N (L) = 0 \text{ } \epsilon / \text{cm}^2
\]
d. Suppose the gate voltage is readjusted so that $V_G - V_T = 3 \text{ V}$. For the new condition, determine $I_D$ if $V_D = 4 \text{ V}$.

$V_D > V_{D-sat} = V_g - V_T \Rightarrow \text{MOSFET is in saturation}$

\[
I_D \approx (V_g - V_T)^2
\]

\[
I_D = \frac{1}{2} I_{D-sat} (V_g - V_T = 3 \text{ V})
\]

\[
1 = \frac{I_{D-sat}}{I_D} = \frac{(V_{g1} - V_T)^2}{(V_{g2} - V_T)^2} = (10^{-3})(\frac{3}{5})^2
\]

\[
I_{D-sat} = 10^{-3} \text{ A (} V_{g2} - V_T = 5 \text{ V)}
\]

\[
I_D = 3.6 \times 10^{-4} \text{ A}
\]

e. If $V_D = 0$ (i.e. the drain is shorted to the source and back), sketch the general shape of $C_G$ (gate capacitance) versus $V_g$ to be expected from the MOSFET.

\[n\text{-channel} \quad \text{low frequency.}\]
Problem # 4:

The most widely encountered MOSFET characteristics are a plot of $I_D$ versus $V_D$ with $V_G$ or $V_G - V_T$ held constant at select values. An alternative plot of $I_D$ versus $V_G$ or $V_G - V_T$ with $V_D$ held constant at select values is sometimes useful. Sketch the shape of the $I_D$ versus $V_G - V_T$ characteristics to be expected from an ideal n-channel MOSFET. Specifically show the characteristics corresponding to $V_D = 1, 2, 3, \text{ and } 4 \text{ V}$. Explain how you arrived at the sketch.

![Graph showing MOSFET characteristics](image)

**Conclusion to note:**

i) Increase $V_G - V_T$ from zero with $V_D = \text{constant}$ initially $V_D > V_G - V_T$ so the device is saturated:

$$I_D = I_D \text{, sat} = \frac{2 \mu_n C}{2L} (V_G - V_T)^2$$

ii) When $V_G - V_T = V_D \rightarrow \text{linear region}$

$$I_D = \frac{2 \mu_n C}{2L} \left[ (V_G - V_T)V_D - V_D^2/2 \right]$$

iii) Increase $V_D \text{ stay on squared part of curve longer } V_G - V_T > V_D$

linear region with increasing slope with increasing $V_D$. 

Problem #5:

Suppose a battery $V_B > 0$ is connected between the gate and drain of an ideal n-channel MOSFET as pictured. Sketch the $I_D$ versus $V_D$ ($V_D > 0$) if $V_B = V_T/2$ and $2 V_T$.

**Condition #1:**

$V_G = V_D + V_B$ or $V_D = V_G - V_B$

In square law theory: $V_D \text{sat} = V_G - V_T$. If $V_B = V_T/2 \Rightarrow V_D = V_G - V_T/2 > V_D \text{sat}$

Therefore the MOSFET is always in saturation. We note $I_D = 0$ if $V_G < V_T$

or if $V_D < V_T/2$:

$$I_D = \frac{2 \mu n C_0}{2L} (V_G - V_T)^2 = \frac{2 \mu n C_0}{2L} (V_D - V_T/2)^2 \quad V_D > V_T/2$$

$$I_D = 0 \quad V_D < V_T/2$$

**Condition #2:**

$V_B = 2 V_T \Rightarrow V_D = V_G - 2V_T < V_G - V_T = V_D \text{sat}$

MOSFET is in the linear regime and turns on for $V_G > V_T$ or $V_D > V_T$ so it is on for all $V_D > 0$

$$I_D = \frac{2 \mu n C_0}{L} \left[ (V_G - V_T) V_D - V_D^2/2 \right] = \frac{2 \mu n C_0}{L} \left[ (V_D + V_T) V_D - V_D^2/2 \right]$$

$$= \frac{2 \mu n C_0}{L} \left( V_D^2/2 + V_T V_D \right) = \frac{2 \mu n C_0}{2L} \left[ (V_D + V_T)^2 - V_T^2 \right] \quad V_D > 0$$
The $\Delta n_E/n_{E0}$, $\Delta p_B/p_{B0}$ and $\Delta n_C/n_{C0}$ distributions in the quasineutral regions of a $pnp$ BJT are shown above.

a. What is the polarity of $V_{EB}$?

$V_{EB} < 0$ as both $\Delta n_E/n_{E0}$ and $\Delta p_B/p_{B0}$ are less than zero at the edge.

b. What is the polarity of $V_{CB}$?

$V_{CB} > 0$ as both $\Delta p_B/p_{B0}$ and $\Delta n_C/n_{C0}$ are greater than zero.

c. What is the magnitude of $V_{CB}$?

$$\Delta p_B (w) = p_{B0} \left( e^{\frac{qV}{kT}} - 1 \right)$$

$$\frac{\Delta p_B (w)}{p_{B0}} = e^{\frac{qV_{cb}}{kT}} - 1 = 10$$

$$V_{cb} = \left( \frac{kT}{q} \right) \ln (10) = 0.062 V$$
Problem #6:

Complete the table below by indicating whether the noted change in a BJT device parameter increases, decreases or has no effect on the listed performance parameters.

<table>
<thead>
<tr>
<th>Change</th>
<th>Effect on ( \gamma )</th>
<th>Effect on ( \alpha )</th>
<th>Effect on ( \beta )</th>
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<td>↓</td>
<td>↓</td>
<td>↓</td>
</tr>
<tr>
<td>Increase ( r_D )</td>
<td>N. C.</td>
<td>↑</td>
<td>↑</td>
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<tr>
<td>Increase ( N_B )</td>
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<tr>
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<td>N. C.</td>
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</tr>
<tr>
<td>Increase ( N_E )</td>
<td>↑</td>
<td>N. C.</td>
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